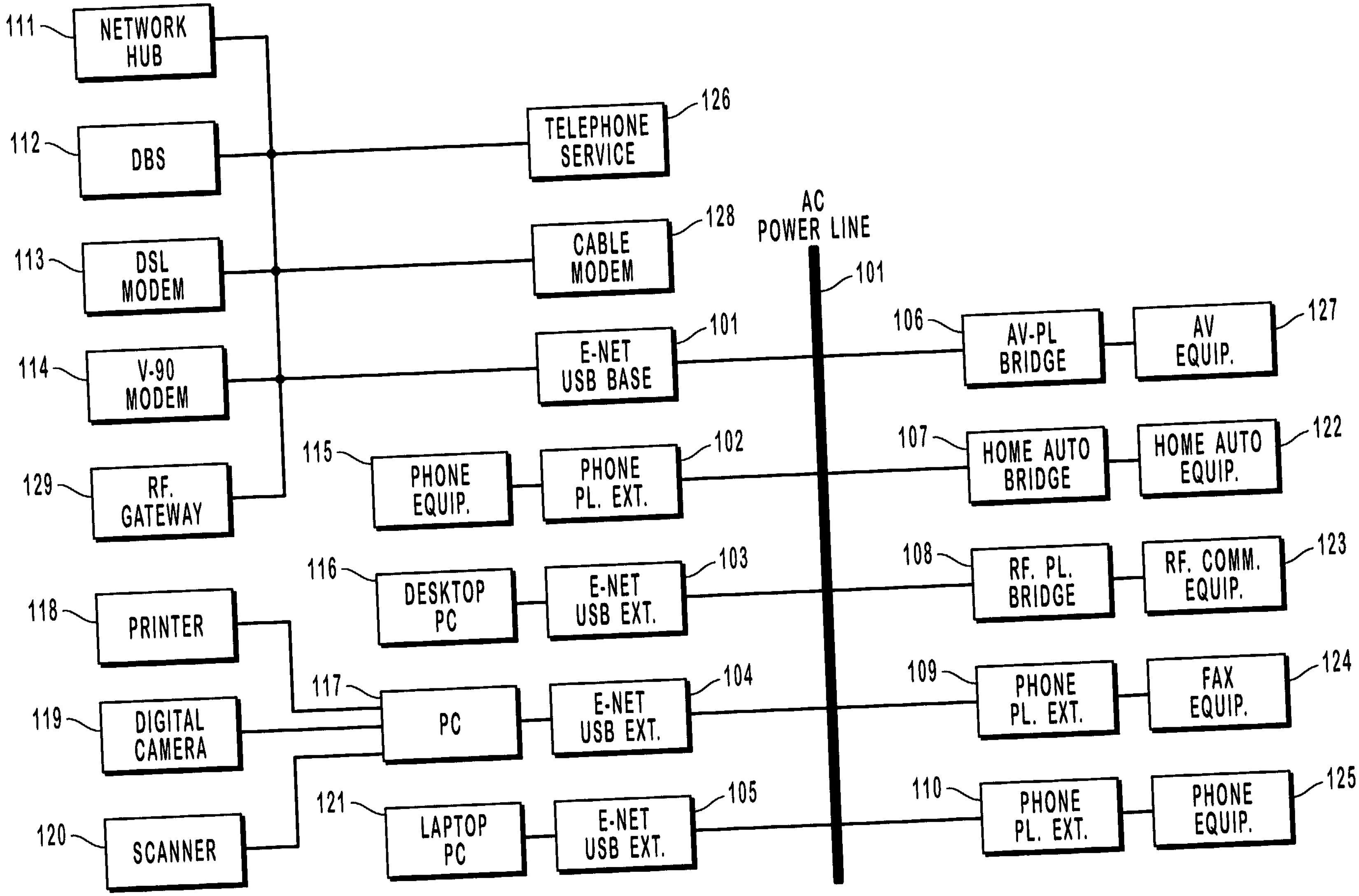

NETWORK HUB
111
DBS
112
DSL MODEM
113
V-90 MODEM
114
RF. GATEWAY
129
TELEPHONE SERVICE
126
CABLE MODEM
128
E-NET USB BASE
101
AC POWER LINE
101
PHONE EQUIP.
115
PHONE PL. EXT.
102
DESKTOP PC
116
E-NET USB EXT.
103
PRINTER
118
DIGITAL CAMERA
119
SCANNER
120
PC
117
E-NET USB EXT.
104
LAPTOP PC
121
E-NET USB EXT.
105
AV-PL BRIDGE
106
AV EQUIP.
127
HOME AUTO BRIDGE
107
HOME AUTO EQUIP.
122
RF. PL. BRIDGE
108
RF. COMM. EQUIP.
123
PHONE PL. EXT.
109
FAX EQUIP.
124
PHONE PL. EXT.
110
PHONE EQUIP.
125

FIG. 1

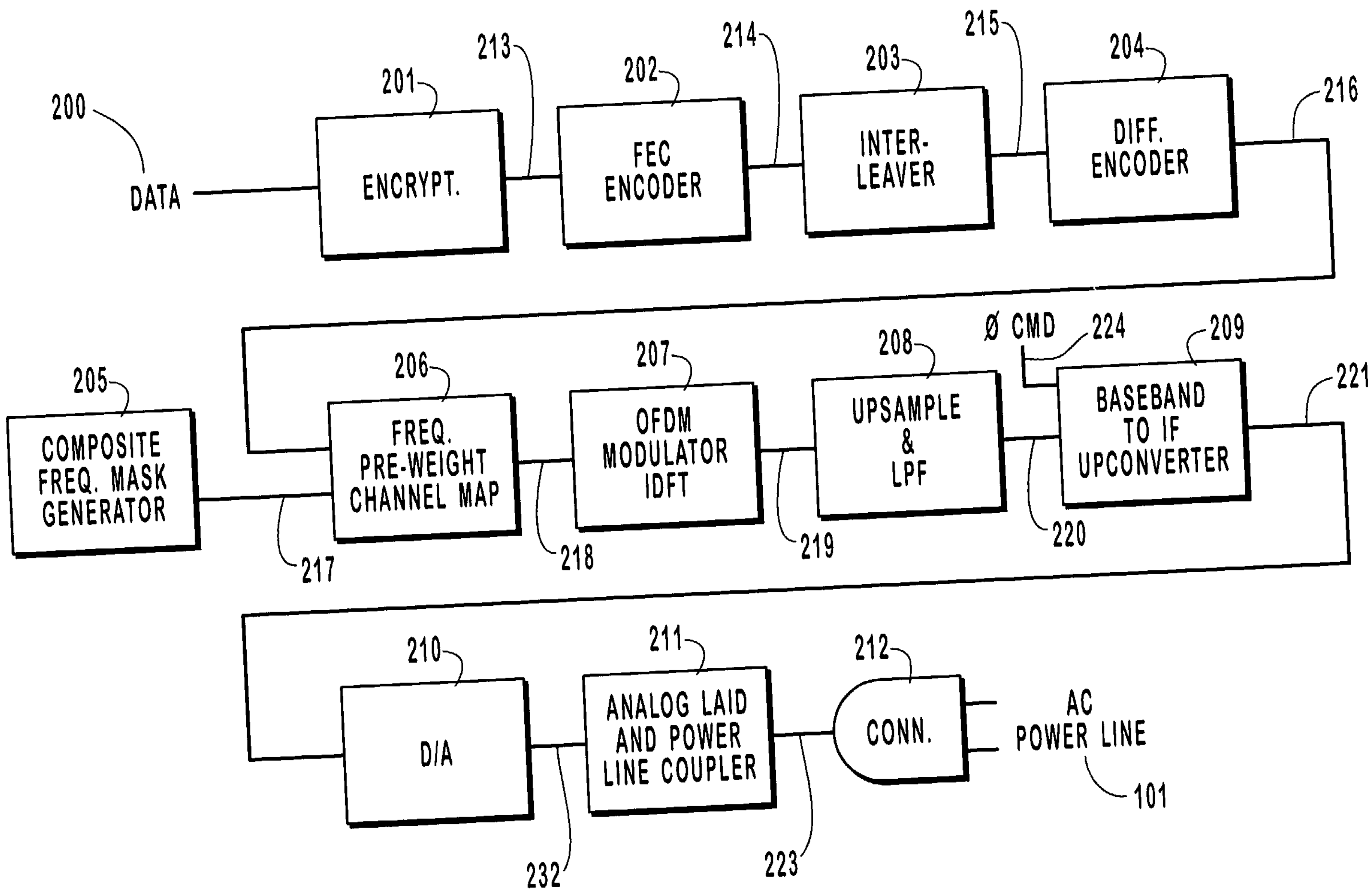

200
DATA
201
ENCRYPT.
213
202
FEC ENCODER
214
203
INTER-LEAVER
215
204
DIFF. ENCODER
216
205
COMPOSITE FREQ. MASK GENERATOR
217
206
FREQ. PRE-WEIGHT CHANNEL MAP
218
207
OFDM MODULATOR IDFT
219
208
UPSAMPLE & LPF
220
Ø CMD
224
209
BASEBAND TO IF UPCONVERTER
221
210
D/A
232
211
ANALOG LAID AND POWER LINE COUPLER
223
212
CONN.
AC POWER LINE
101

FIG. 2

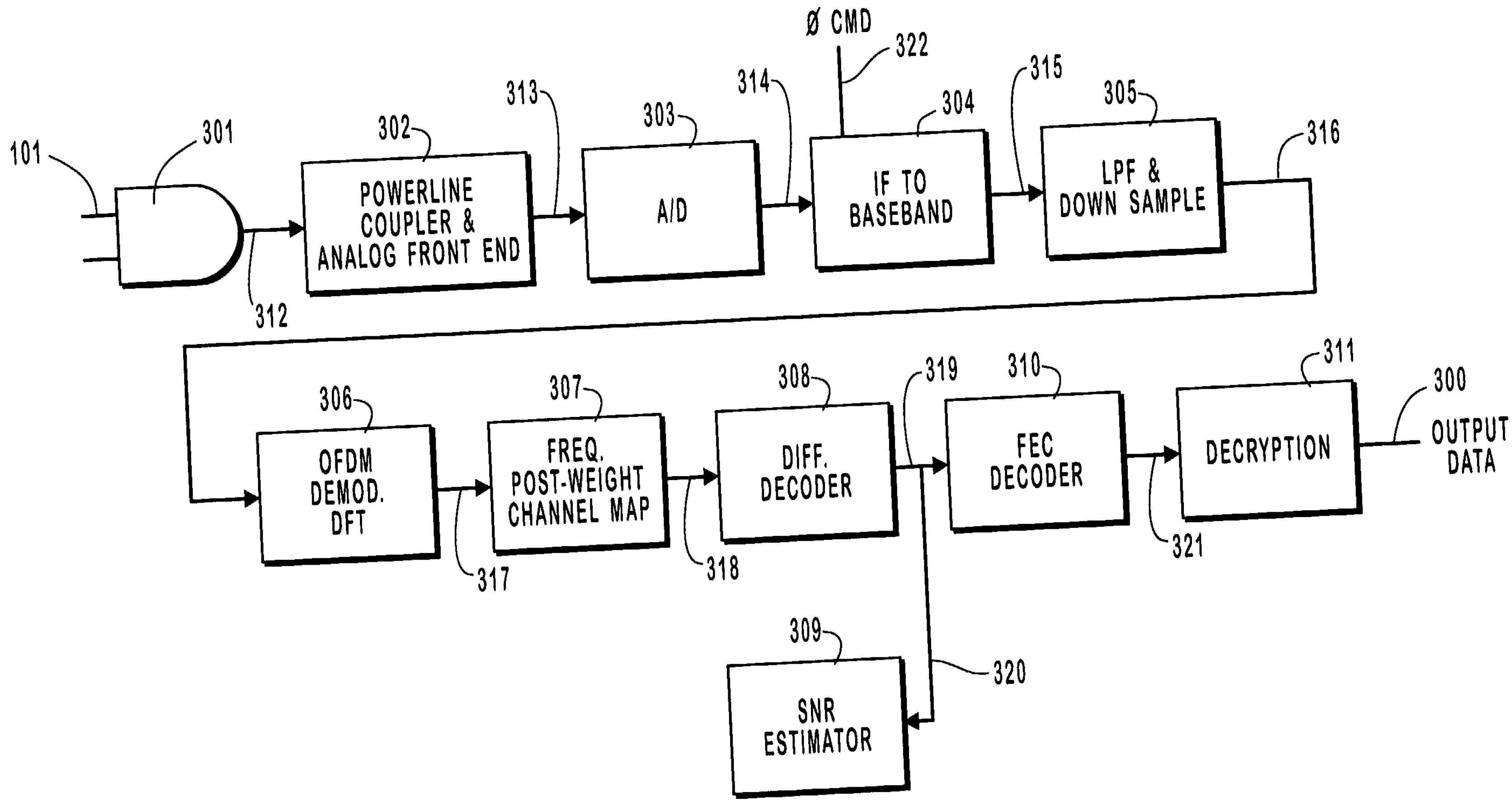

101
301
312
302
POWERLINE
COUPLER &
ANALOG FRONT END
313
303
A/D
314
Ø CMD
322
304
IF TO
BASEBAND
315
305
LPF &
DOWN SAMPLE
316
306
OFDM
DEMOD.
DFT
317
307
FREQ.
POST-WEIGHT
CHANNEL MAP
318
308
DIFF.
DECODER
319
310
FEC
DECODER
321
311
DECRYPTION
300
OUTPUT
DATA
309
SNR
ESTIMATOR
320

FIG. 3

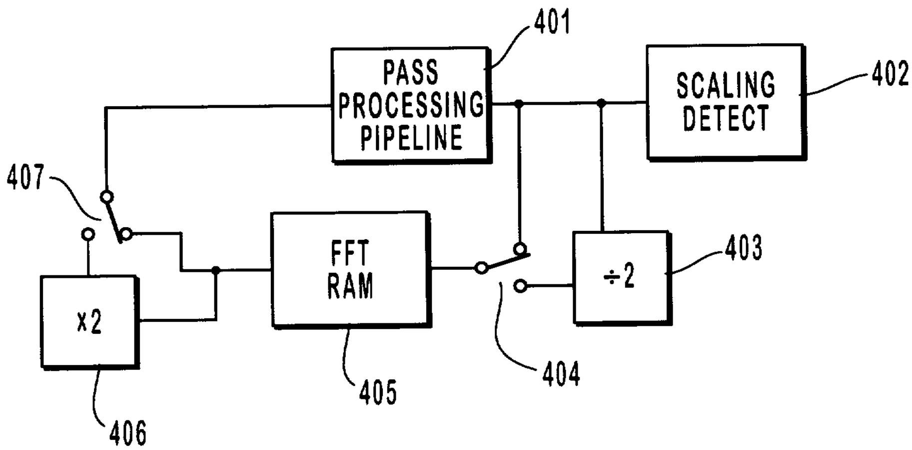

401
PASS PROCESSING PIPELINE
SCALING DETECT
402
407
FFT RAM
÷2
403
x2
405
404
406

FIG. 4

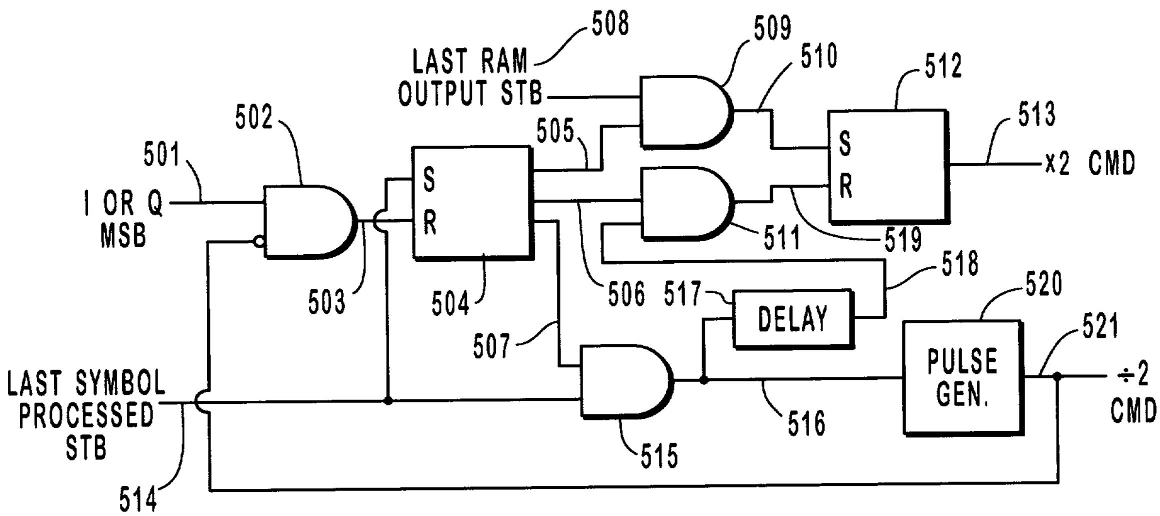

508
LAST RAM OUTPUT STB
509
510
512
502
501
505
513
I OR Q MSB
S
R
S
R
x2 CMD
511
519
503
504
506
517
518
DELAY
520
507
521
LAST SYMBOL PROCESSED STB
PULSE GEN.
÷2 CMD
516
515
514

FIG. 5

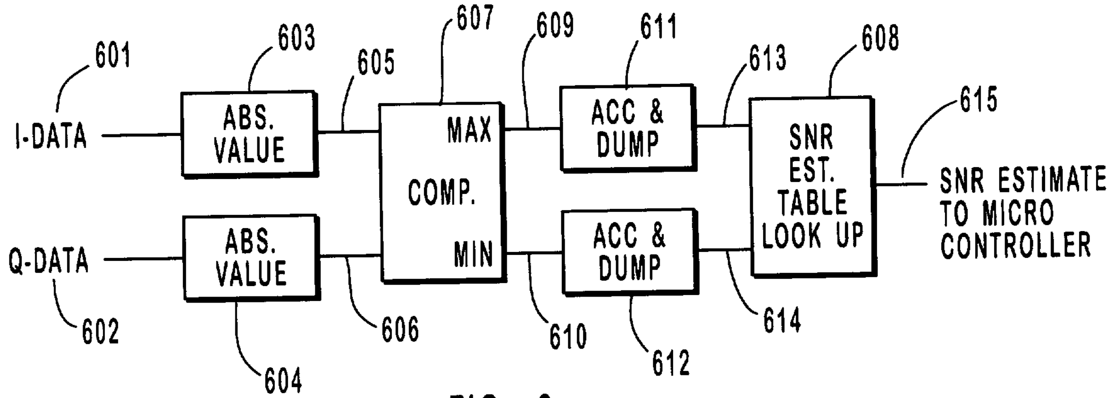


FIG. 6

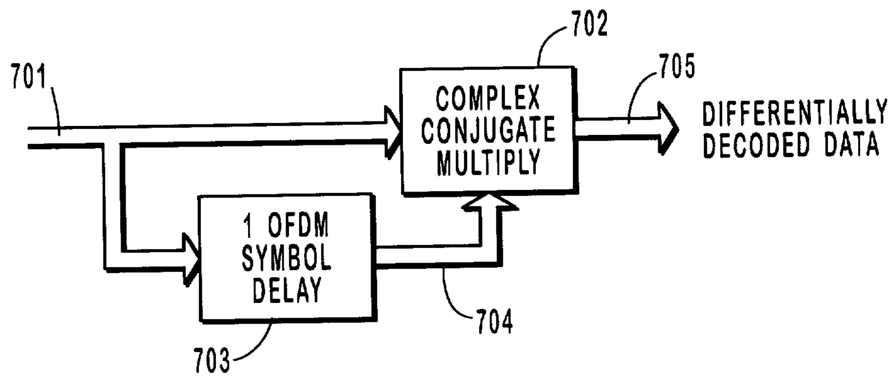


FIG. 7

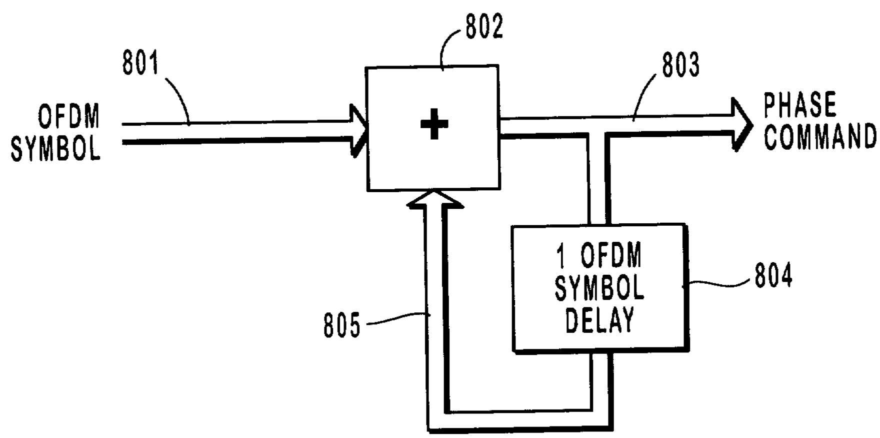


FIG. 8

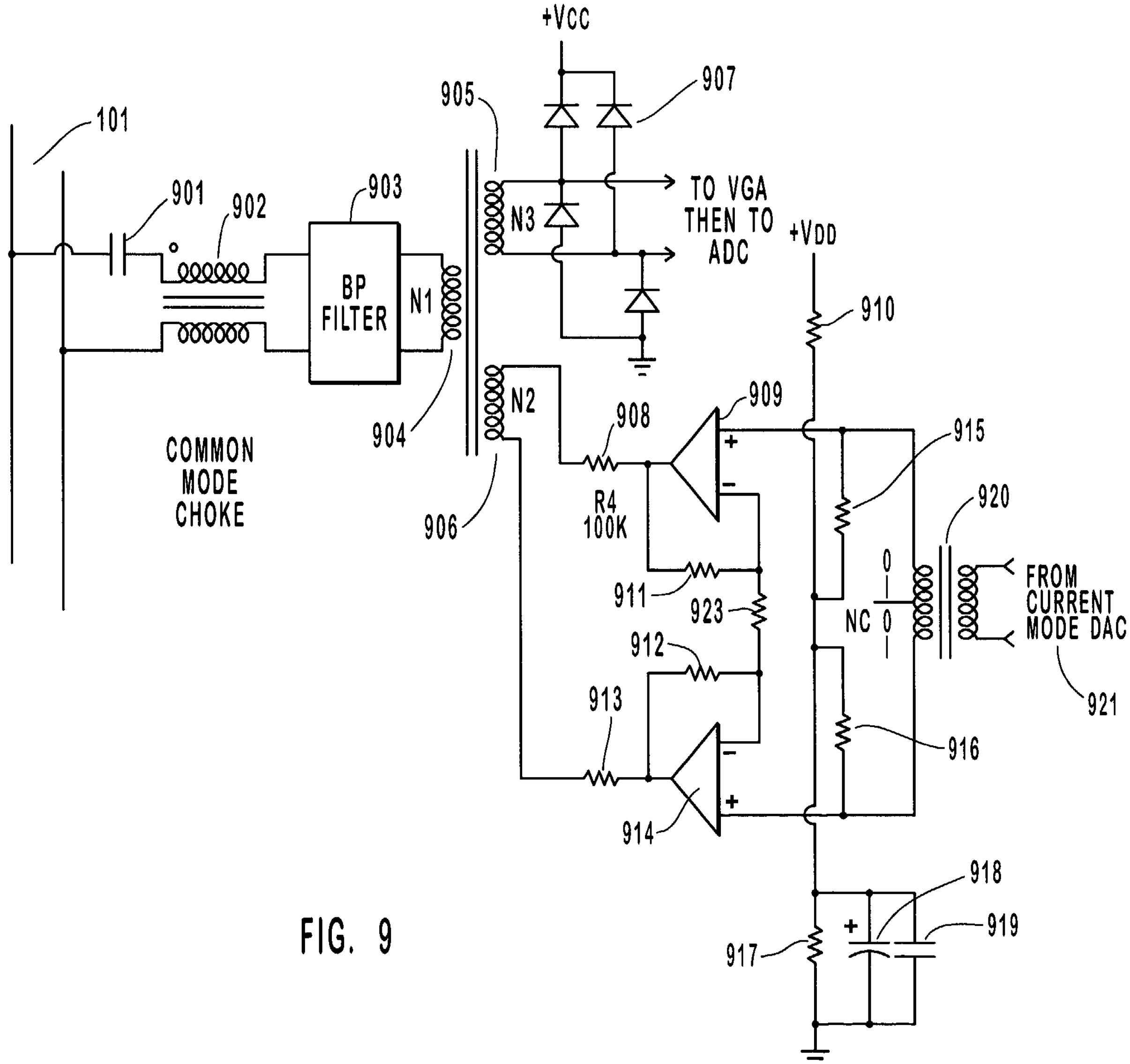

101
901
902
COMMON
MODE
CHOKE
903
BP
FILTER
N1
904
905
906
N3
N2
+VCC
907
TO VGA
THEN TO
ADC
+VDD
910
908
R4
100K
909
911
923
912
913
914
915
916
920
0
NC
0
FROM
CURRENT
MODE DAC
921
917
918
919

FIG. 9

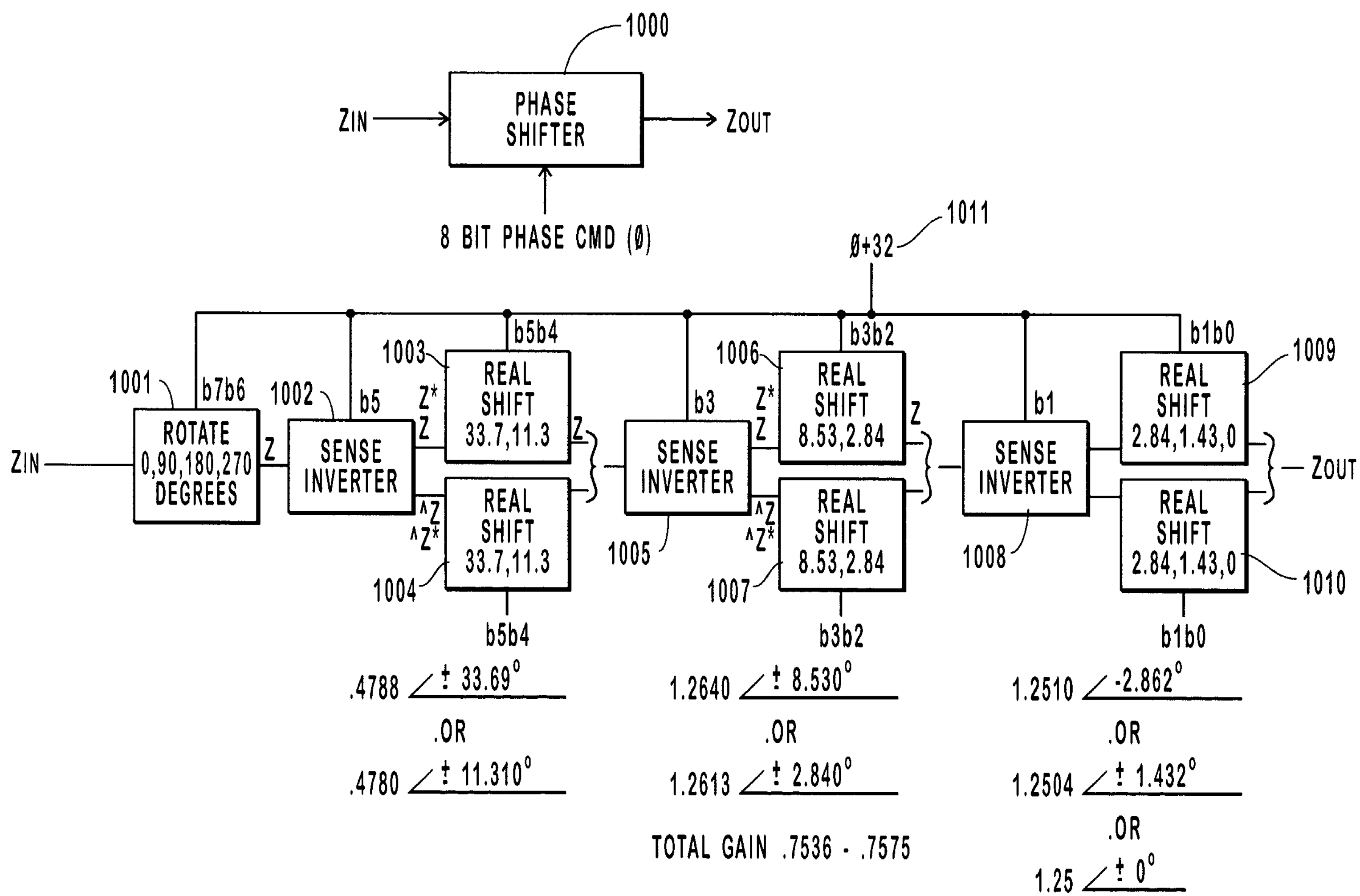
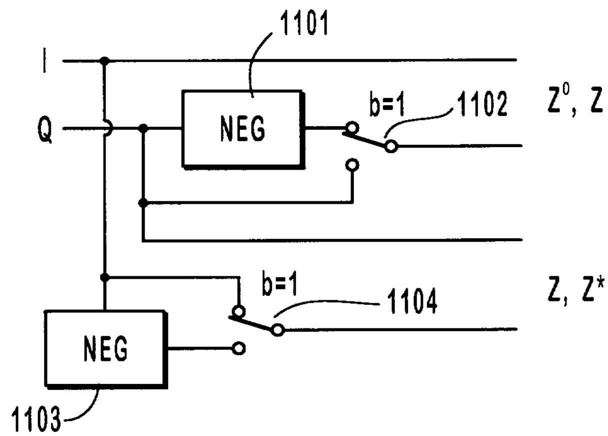
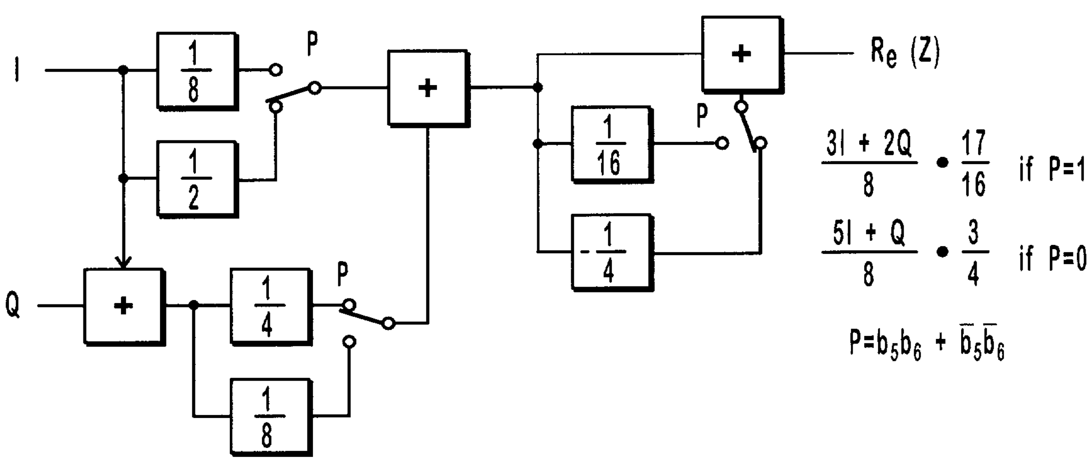

1000
ZIN
PHASE SHIFTER
ZOUT
8 BIT PHASE CMD (Ø)
Ø+32
1011
ZIN
1001
ROTATE 0,90,180,270 DEGREES
b7b6
Z
1002
SENSE INVERTER
b5
1003
Z*
Z
REAL SHIFT 33.7,11.3
b5b4
^Z
^Z*
1004
REAL SHIFT 33.7,11.3
b5b4
Z
SENSE INVERTER
b3
1005
1006
Z*
Z
REAL SHIFT 8.53,2.84
b3b2
^Z
^Z*
1007
REAL SHIFT 8.53,2.84
b3b2
Z
SENSE INVERTER
b1
1008
REAL SHIFT 2.84,1.43,0
b1b0
1009
REAL SHIFT 2.84,1.43,0
b1b0
1010
ZOUT
.4788 ∠ ± 33.69°
.OR
.4780 ∠ ± 11.310°
1.2640 ∠ ± 8.530°
.OR
1.2613 ∠ ± 2.840°
1.2510 ∠ -2.862°
.OR
1.2504 ∠ ± 1.432°
.OR
1.25 ∠ ± 0°
TOTAL GAIN .7536 - .7575

FIG. 10



1101
I
Q
NEG
b=1
1102
Z^{0}, Z
b=1
1104
Z, Z*
NEG
1103

FIG. 11



I
$\frac{1}{8}$
P
+
$\frac{1}{2}$
Q
+
$\frac{1}{4}$
P
$\frac{1}{8}$
$\frac{1}{16}$
P
$-\frac{1}{4}$
+
Re (Z)
$\frac{3I + 2Q}{8} \bullet \frac{17}{16}$ if P=1
$\frac{5I + Q}{8} \bullet \frac{3}{4}$ if P=0
$P = b_5 b_6 + \overline{b_5}\,\overline{b_6}$

FIG. 12

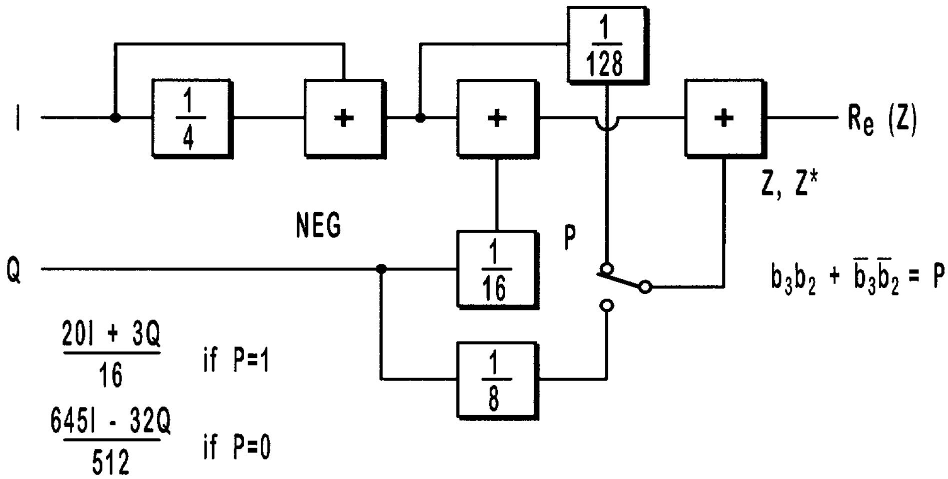
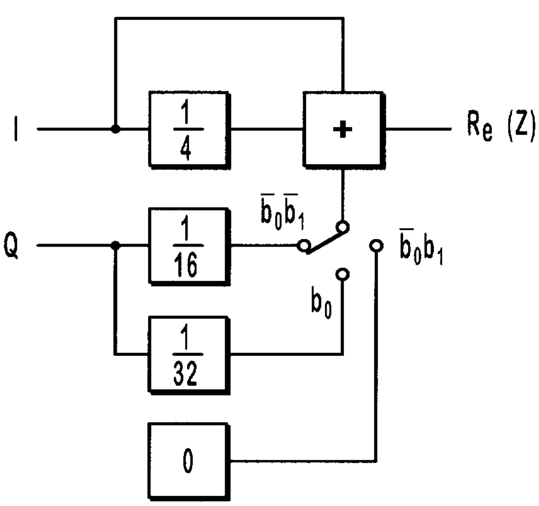


FIG. 13



$\frac{20I + Q}{16}$ if $\bar{b}_0\bar{b}_1$

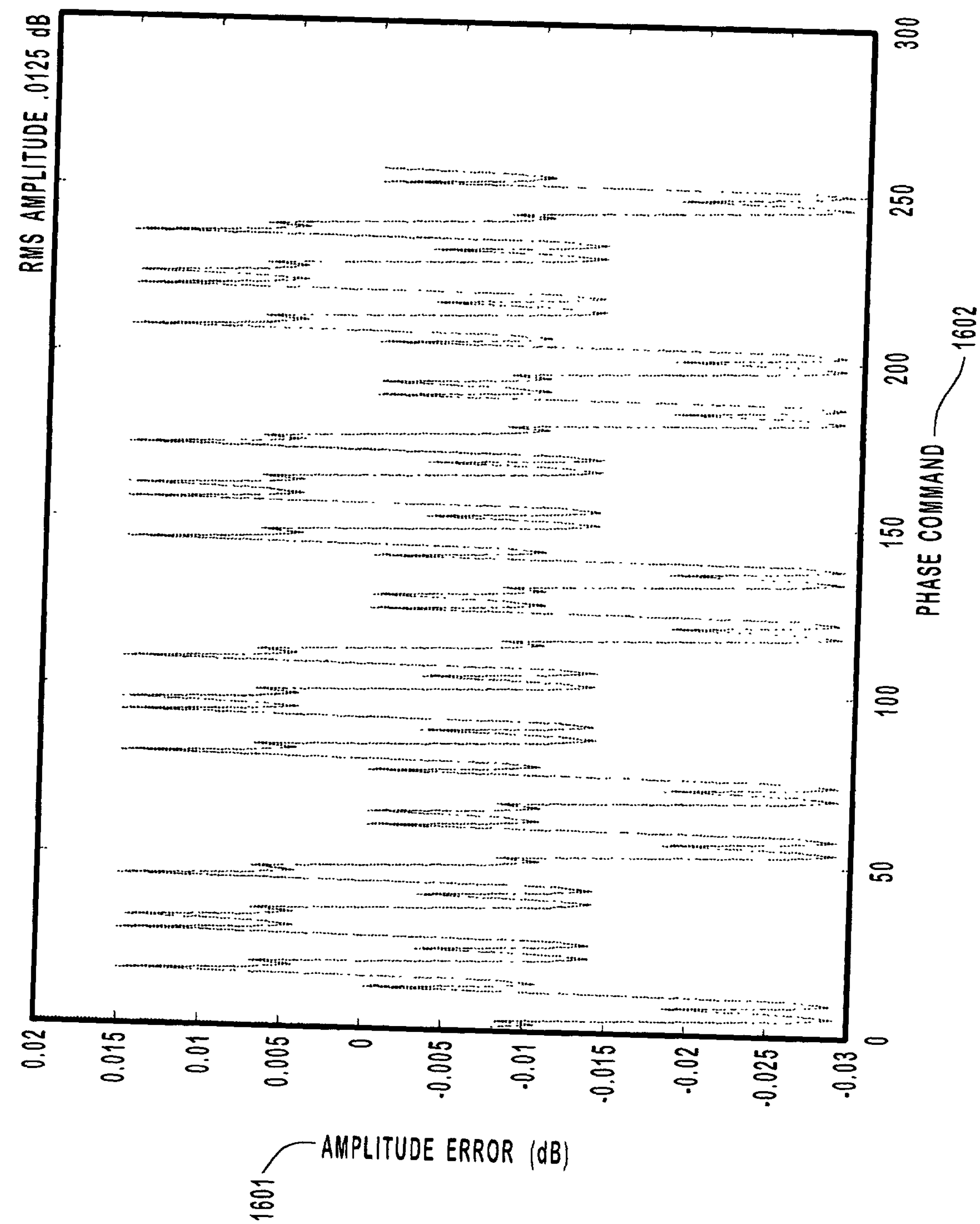
$\frac{40I + Q}{32}$ if b_0

$\frac{5I}{4}$ if $\bar{b}_0 b_1$

FIG. 14

```
function z= pshift1(z,th);
iz=real(z); qz=imag(z);
tha=2*(bitand(th+32,2.^(0:7))>0)-1; %make array of phase bits + 32

%0,90,180,270
if tha(7)= =1;z=j*z;end;
if tha(8)= =1;z= -z; end;

% + - 33.69,11.31
if tha(6)*tha(5)= = -1;
        z=3/16*(5+tha(6)*j)*z;
else;
        z=17/64*(3+tha(6)*2*j)*z;
end;

% +- 8.53,2.84
if tha(4)*tha(3)= =-1;
        z=(20*(1+1/128) + tha(4)*j)*z/32;
else;
        z=(20+tha(4)*3*j)*z/32;
end;

% -2.86 –1.43 0 1.43
if tha(1)= =1;
        z=(40+tha(2)*j)*z/32;
elseif tha(2)= = -1;
        z=(20-j)*z/16;
else;
        z=5*z/4;
end;
```

FIG. 15



RMS AMPLITUDE .0125 dB
AMPLITUDE ERROR (dB)
1601
0.02
0.015
0.01
0.005
0
-0.005
-0.01
-0.015
-0.02
-0.025
-0.03
0
50
100
150
200
250
300
PHASE COMMAND
1602

FIG. 16

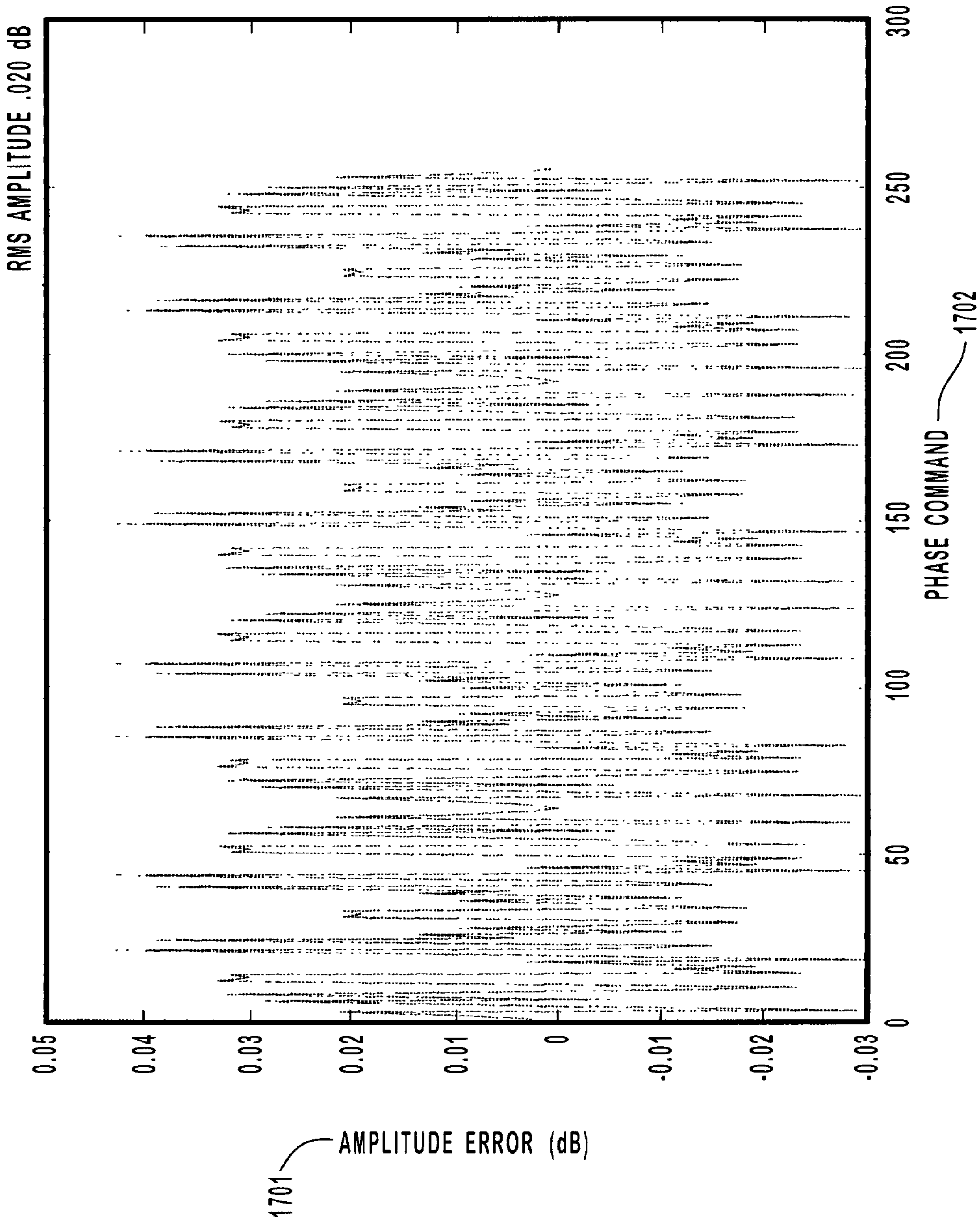

RMS AMPLITUDE .020 dB
AMPLITUDE ERROR (dB)
1701
0.05
0.04
0.03
0.02
0.01
0
-0.01
-0.02
-0.03
PHASE COMMAND
1702
0
50
100
150
200
250
300

FIG. 17

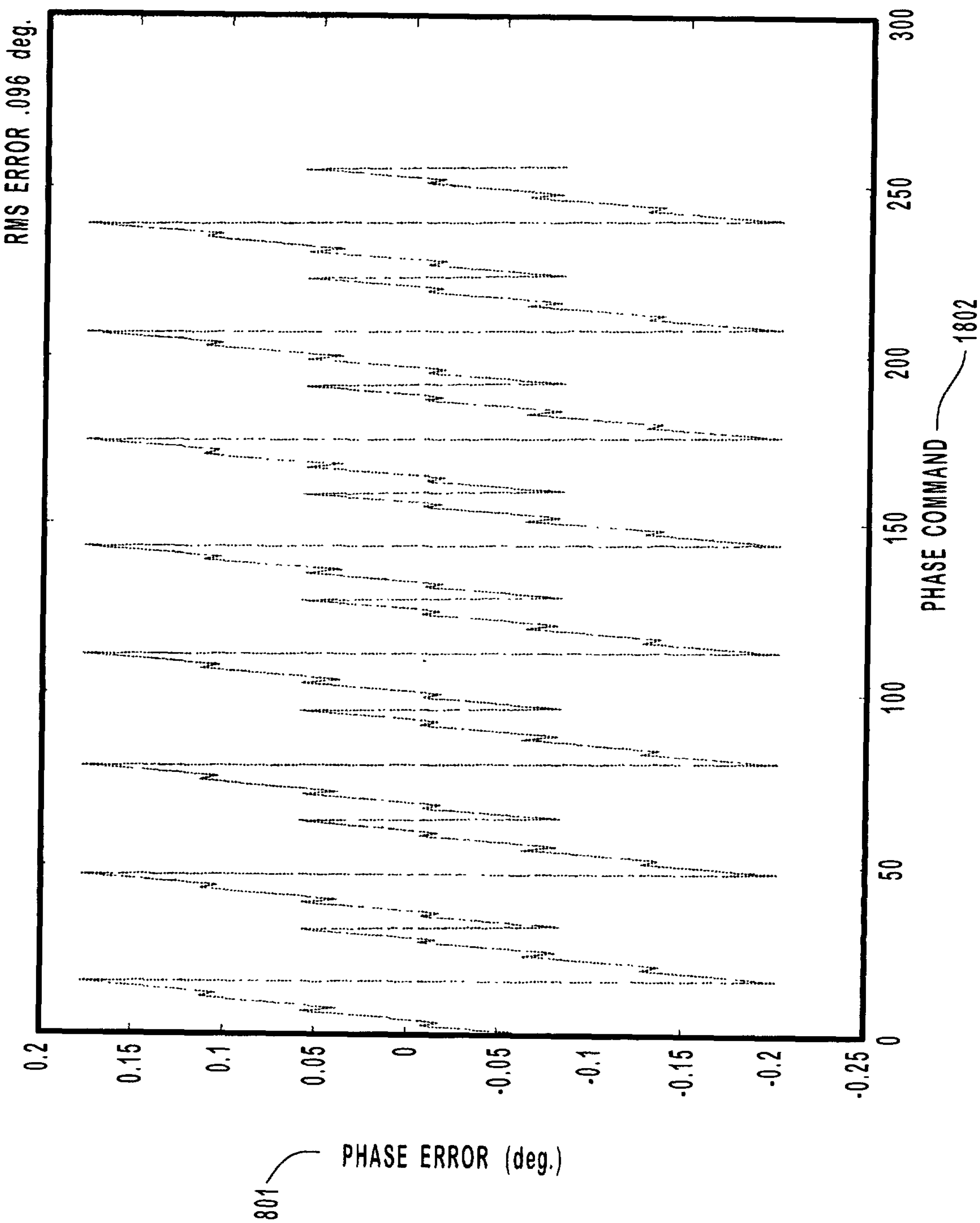

RMS ERROR .096 deg.
PHASE ERROR (deg.)
1801
PHASE COMMAND
1802
0.2
0.15
0.1
0.05
0
-0.05
-0.1
-0.15
-0.2
-0.25
0
50
100
150
200
250
300

FIG. 18

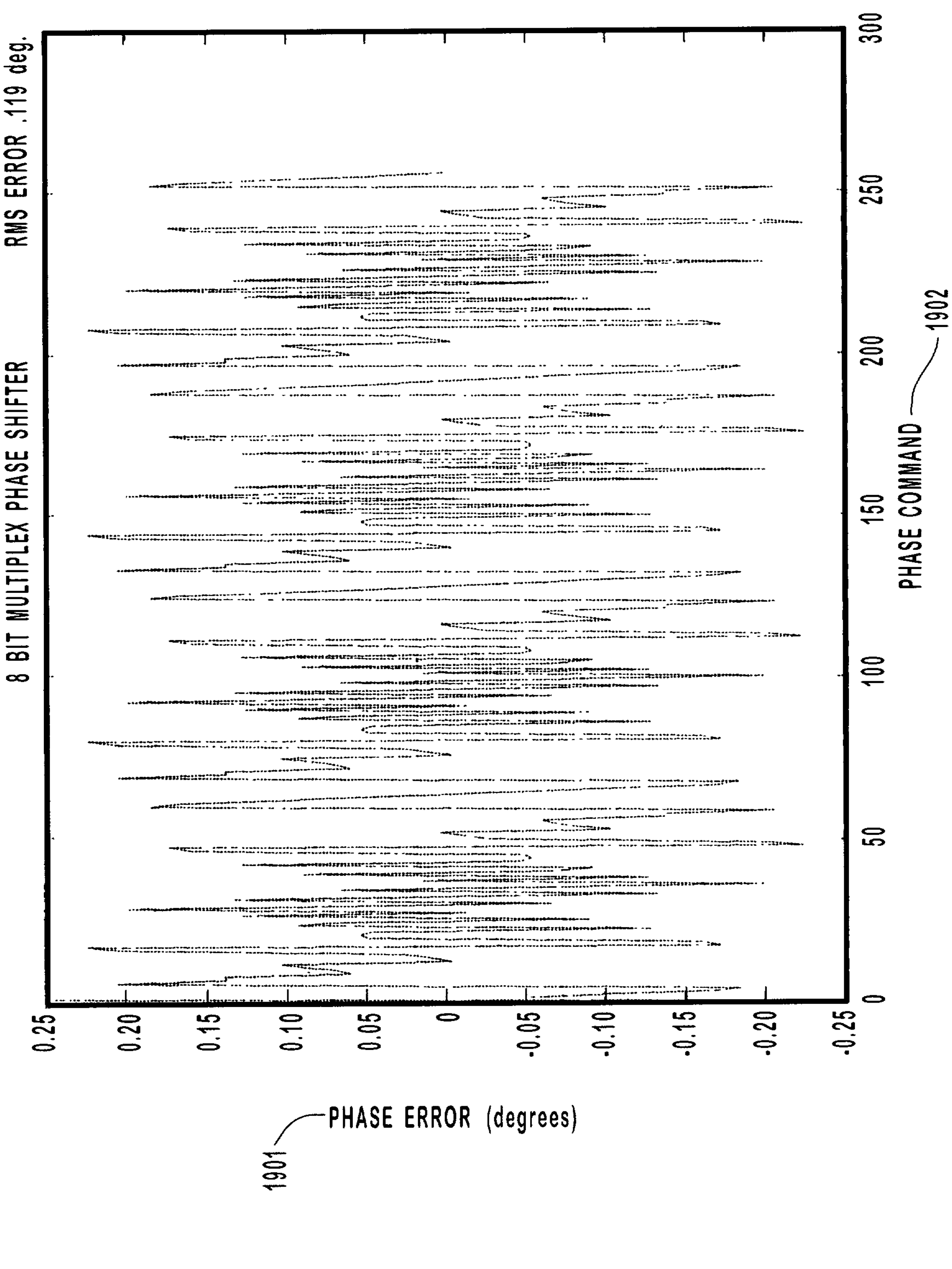

8 BIT MULTIPLEX PHASE SHIFTER
RMS ERROR .119 deg.
PHASE ERROR (degrees)
1901
0.25
0.20
0.15
0.10
0.05
0
-0.05
-0.10
-0.15
-0.20
-0.25
0
50
100
150
200
250
300
PHASE COMMAND
1902

FIG. 19

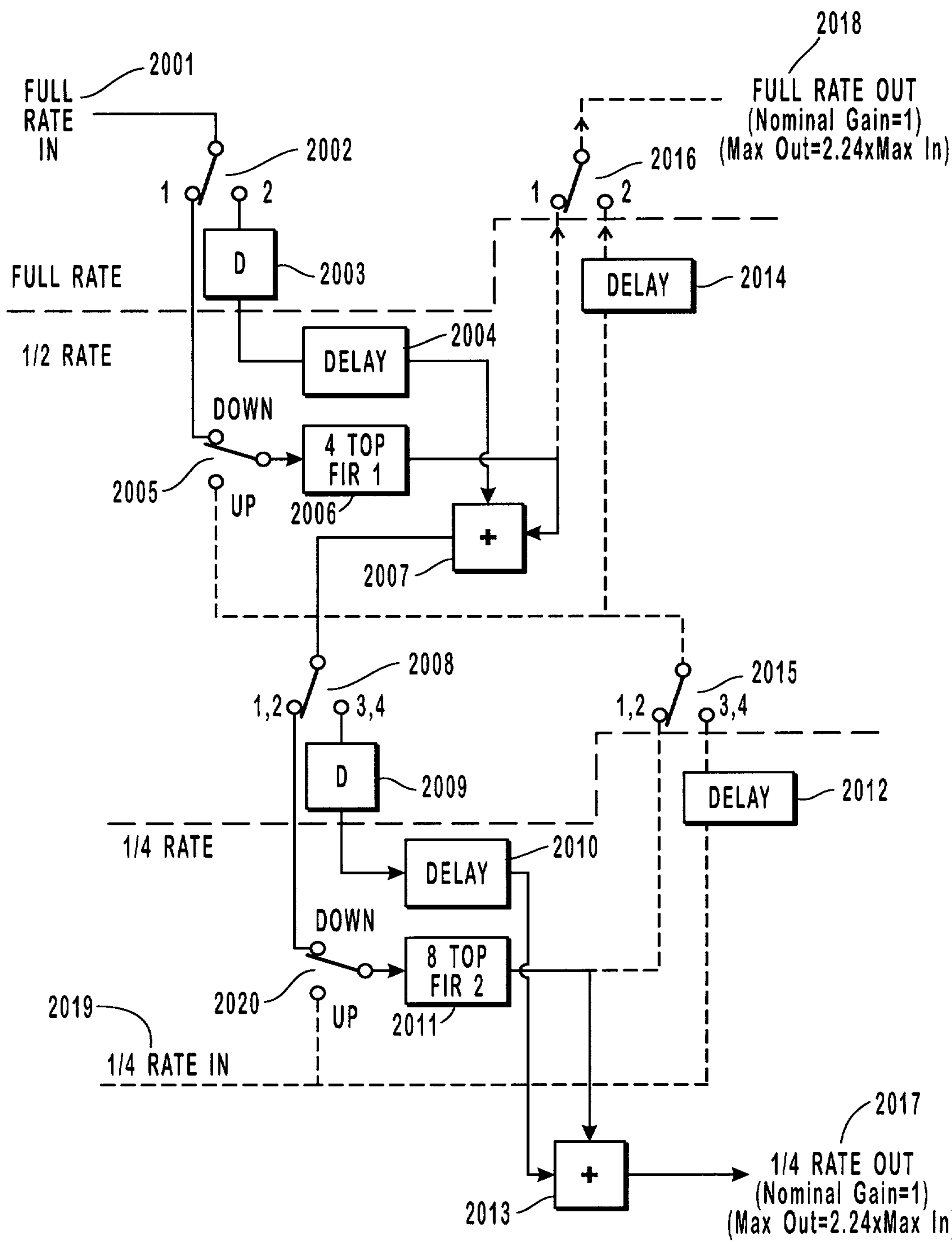
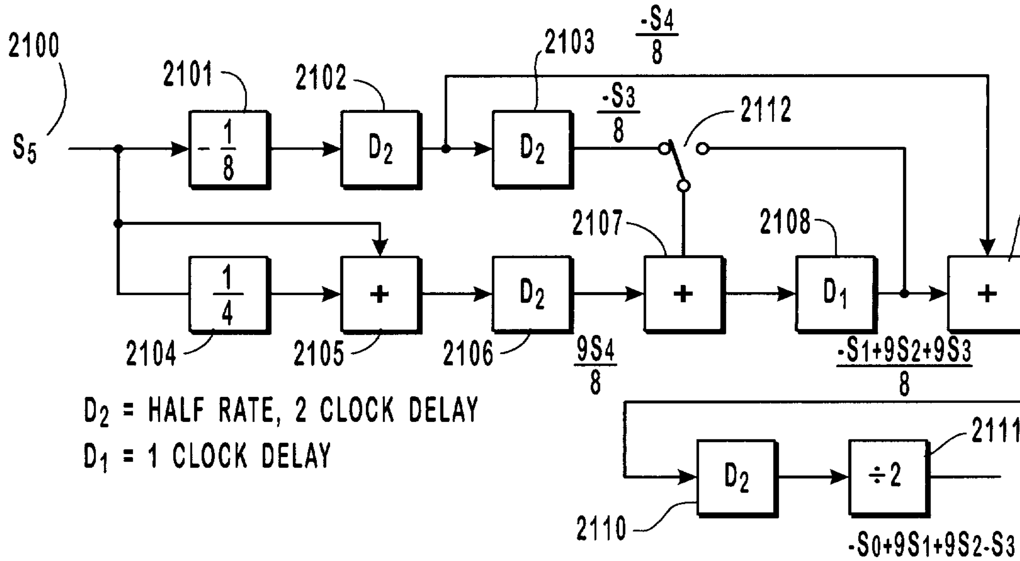
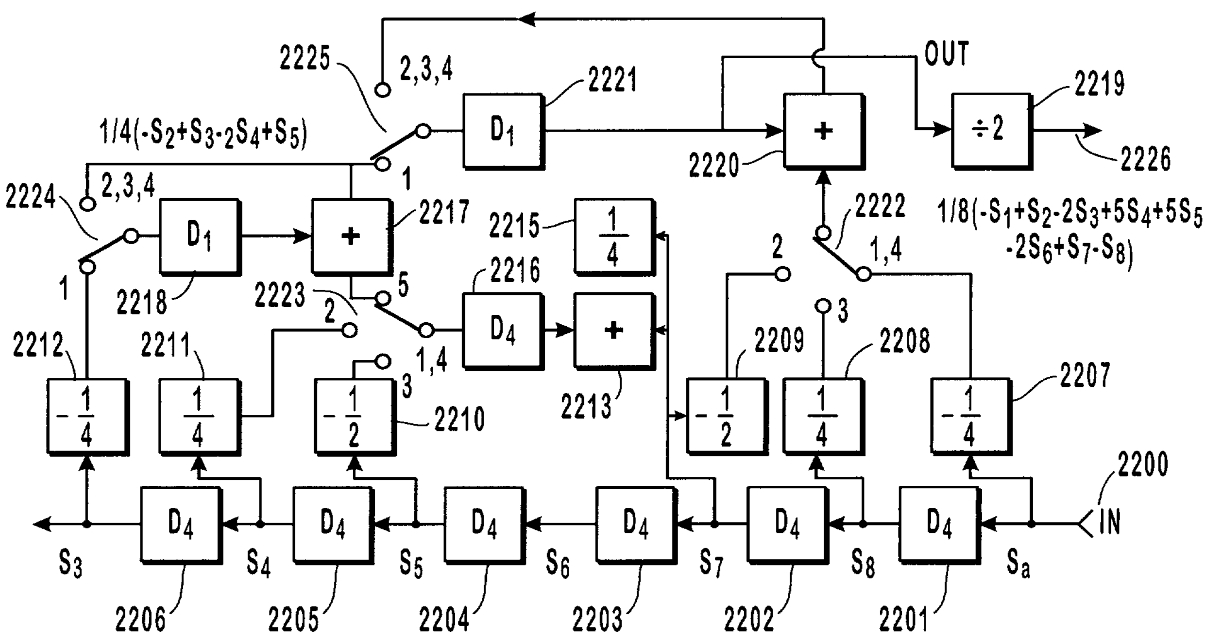

2001
FULL RATE IN
2002
1
2
D
2003
FULL RATE
1/2 RATE
DELAY
2004
DOWN
4 TOP FIR 1
2005
UP
2006
+
2007
2016
1
2
DELAY
2014
2018
FULL RATE OUT
(Nominal Gain=1)
(Max Out=2.24xMax In)
2008
1,2
3,4
D
2009
1/4 RATE
DELAY
2010
DOWN
8 TOP FIR 2
2020
UP
2011
2019
1/4 RATE IN
2015
1,2
3,4
DELAY
2012
+
2013
2017
1/4 RATE OUT
(Nominal Gain=1)
(Max Out=2.24xMax In)

FIG. 20



2100
S5
2101
- 1/8
2102
D2
2103
D2
-S4/8
-S3/8
2112
2107
2108
2109
1/4
+
D2
+
D1
+
2104
2105
2106
9S4/8
-S1+9S2+9S3/8
D2 = HALF RATE, 2 CLOCK DELAY
D1 = 1 CLOCK DELAY
D2
÷2
2111
2110
-S0+9S1+9S2-S3

FIG. 21



2225
2,3,4
D1
2221
OUT
+
÷2
2219
1/4(-S2+S3-2S4+S5)
1
2220
2226
2224
2,3,4
D1
+
2217
2215
1/4
2222
1/8(-S1+S2-2S3+5S4+5S5
-2S6+S7-S8)
2
1,4
1
2218
2223
5
2216
D4
+
3
2212
2211
2
1,4
2213
2209
2208
2207
- 1/4
1/4
- 1/2
3
2210
- 1/2
1/4
- 1/4
2200
D4
D4
D4
D4
D4
D4
IN
S3
S4
S5
S6
S7
S8
Sa
2206
2205
2204
2203
2202
2201

FIG. 22

Anatomy of the FFT

This is a 256 point base 2 example of an FFT (a fast dft)

$k := 0..255$ FFT index

$x_k := \mathrm{rnd}(1) + j \cdot \mathrm{rnd}(1)$ FFT dummy arguement

The discfrete forrier transform takes 256 ^2 operations

$$DFT_k := \sum_{i=0}^{255} x_i \cdot e^{j \cdot 2 \cdot \pi \cdot \frac{i \cdot k}{256}}$$

If we combine terms from the first and 2nd half of the summation we have

$$\sum_{i=0}^{127} \left(x_i + x_{i+128} \cdot e^{j \cdot 2 \cdot \pi \cdot \frac{k}{2}} \right) \cdot e^{j \cdot 2 \cdot \pi \cdot \frac{i \cdot k}{256}}$$

Note the term in paremphases runs over half of N and is only unique for k mod 2 so:

$i1 := 0..127 \qquad k1 := 0..1$

$$X1_{i1,k1} := x_{i1} + x_{i1+128} \cdot e^{(j \cdot 2 \cdot \pi) \cdot \frac{k1}{2}}$$

Then

$$DFT1_k := \sum_{i=0}^{127} X1_{i,\mathrm{mod}(k,2)} \cdot e^{j \cdot 2 \cdot \pi \cdot \frac{i \cdot k}{256}} \qquad \sum_k \left(\left| DFT_k - DFT1_k \right| \right)^2 = 0$$

This operation only takes half the DFT steps by taking 128 steps to precompute X1

We can further reduce the computational load by doing the same thing again

$i1 := 0..63 \qquad k1 := 0..3$

$$X2_{i1,k1} := X1_{i1,\mathrm{mod}(k1,2)} + X1_{i1+64,\mathrm{mod}(k1,2)} \cdot e^{(j \cdot 2 \cdot \pi) \cdot \frac{k1}{4}}$$

Then

$$DFT2_k := \sum_{i=0}^{63} X2_{i,\mathrm{mod}(k,4)} \cdot e^{j \cdot 2 \cdot \pi \cdot \frac{i \cdot k}{256}} \qquad \sum_k \left(\left| DFT_k - DFT2_k \right| \right)^2 = 0$$

FIG. 23a

We repeat this operation a total of 8 times until i ranges only over zero
We show one more trick. Instead of:

$$i1 := 0 .. 31 \qquad k1 := 0 .. 7$$

$$X3_{i1,k1} := X2_{i1,\mathrm{mod}(k1,4)} + X2_{i1+32,\mathrm{mod}(k1,4)} \cdot e^{(j \cdot 2\cdot\pi)\frac{k1}{8}}$$

Use

$$k1 := 0 .. 3 \qquad t_{i1,k1} := X2_{i1+32,k1} \cdot e^{(j \cdot 2\cdot\pi)\frac{k1}{8}}$$

$$X3_{i1,k1} := X2_{i1,k1} + t_{i1,k1} \qquad X3_{i1,k1+4} := X2_{i1,k1} - t_{i1,k1}$$

It only requires half the phase shifts. This operation is called a **butterfly**
Continuing

$$i1 := 0 .. 15 \qquad k1 := 0 .. 7 \qquad t_{i1,k1} := X3_{i1+16,k1} \cdot e^{(j \cdot 2\cdot\pi)\frac{k1}{16}}$$

$$X4_{i1,k1} := X3_{i1,k1} + t_{i1,k1} \qquad X4_{i1,k1+8} := X3_{i1,k1} - t_{i1,k1}$$

$$i1 := 0 .. 7 \qquad k1 := 0 .. 15 \qquad t_{i1,k1} := X4_{i1+8,k1} \cdot e^{(j \cdot 2\cdot\pi)\frac{k1}{32}}$$

$$X5_{i1,k1} := X4_{i1,k1} + t_{i1,k1} \qquad X5_{i1,k1+16} := X4_{i1,k1} - t_{i1,k1}$$

$$i1 := 0 .. 3 \qquad k1 := 0 .. 31 \qquad t_{i1,k1} := X5_{i1+4,k1} \cdot e^{(j \cdot 2\cdot\pi)\frac{k1}{64}}$$

$$X6_{i1,k1} := X5_{i1,k1} + t_{i1,k1} \qquad X6_{i1,k1+32} := X5_{i1,k1} - t_{i1,k1}$$

$$i1 := 0 .. 1 \qquad k1 := 0 .. 63 \qquad t_{i1,k1} := X6_{i1+2,k1} \cdot e^{(j \cdot 2\cdot\pi)\frac{k1}{128}}$$

$$X7_{i1,k1} := X6_{i1,k1} + t_{i1,k1} \qquad X7_{i1,k1+64} := X6_{i1,k1} - t_{i1,k1}$$

and finally

$$k1 := 0 .. 127 \qquad t_{0,k1} := X7_{1,k1} \cdot e^{(j \cdot 2\cdot\pi)\frac{k1}{256}}$$

$$X8_{k1} := X7_{0,k1} + t_{0,k1} \qquad X8_{k1+128} := X7_{0,k1} - t_{0,k1}$$

$$\sum_{k} \left(\left| DFT_k - X8_k \right| \right)^2 = 0$$

FIG. 23b

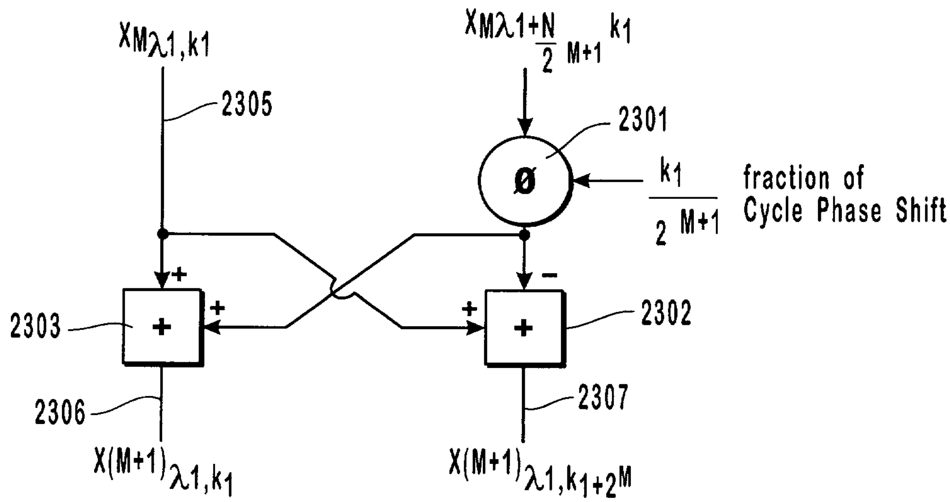


FIG. 23c

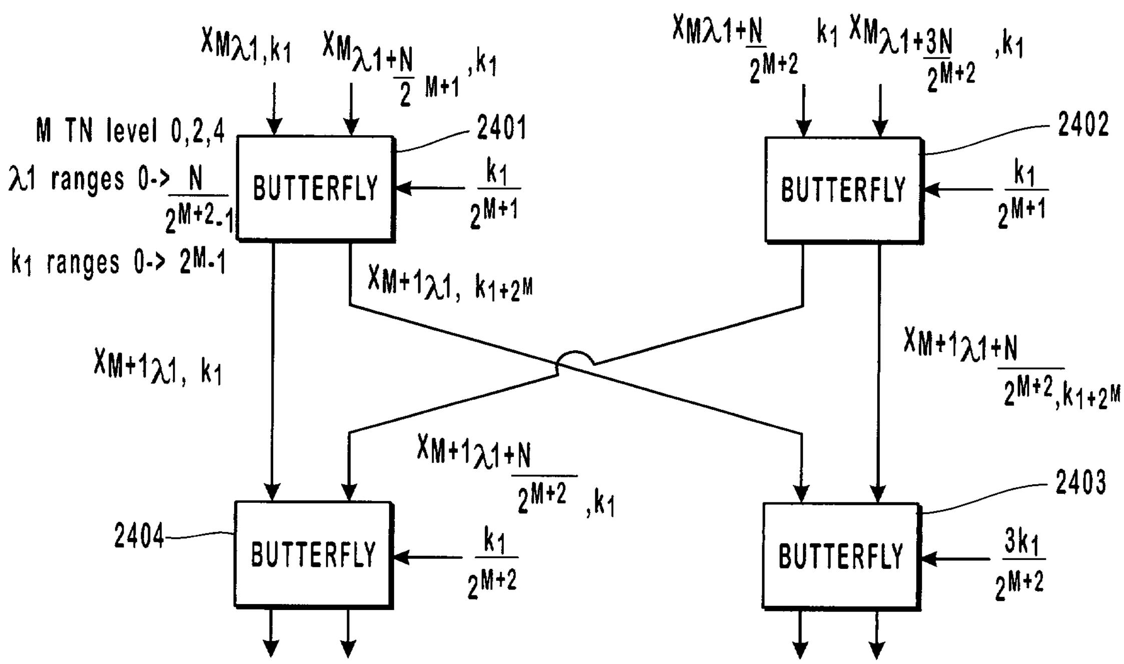


FIG. 24

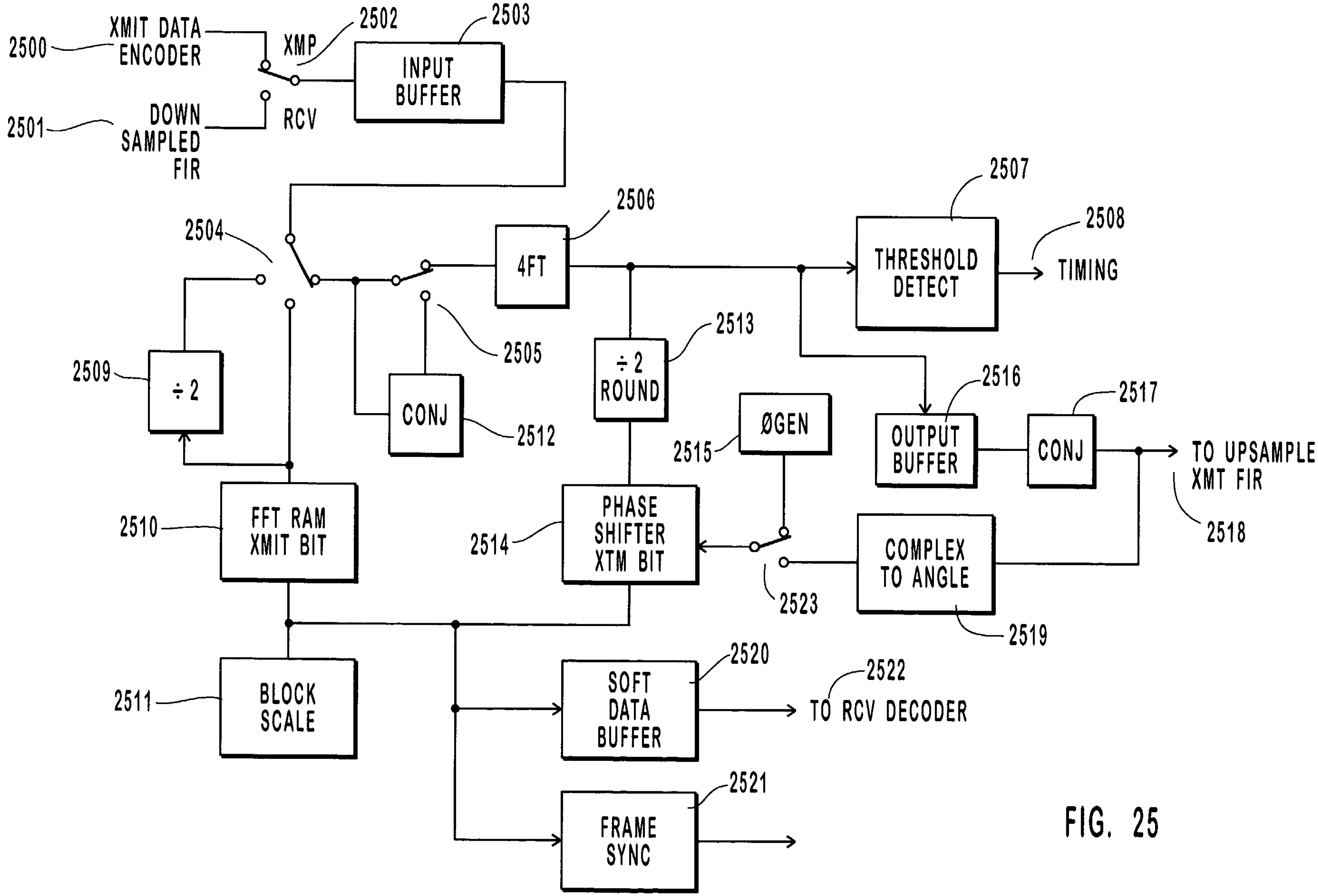
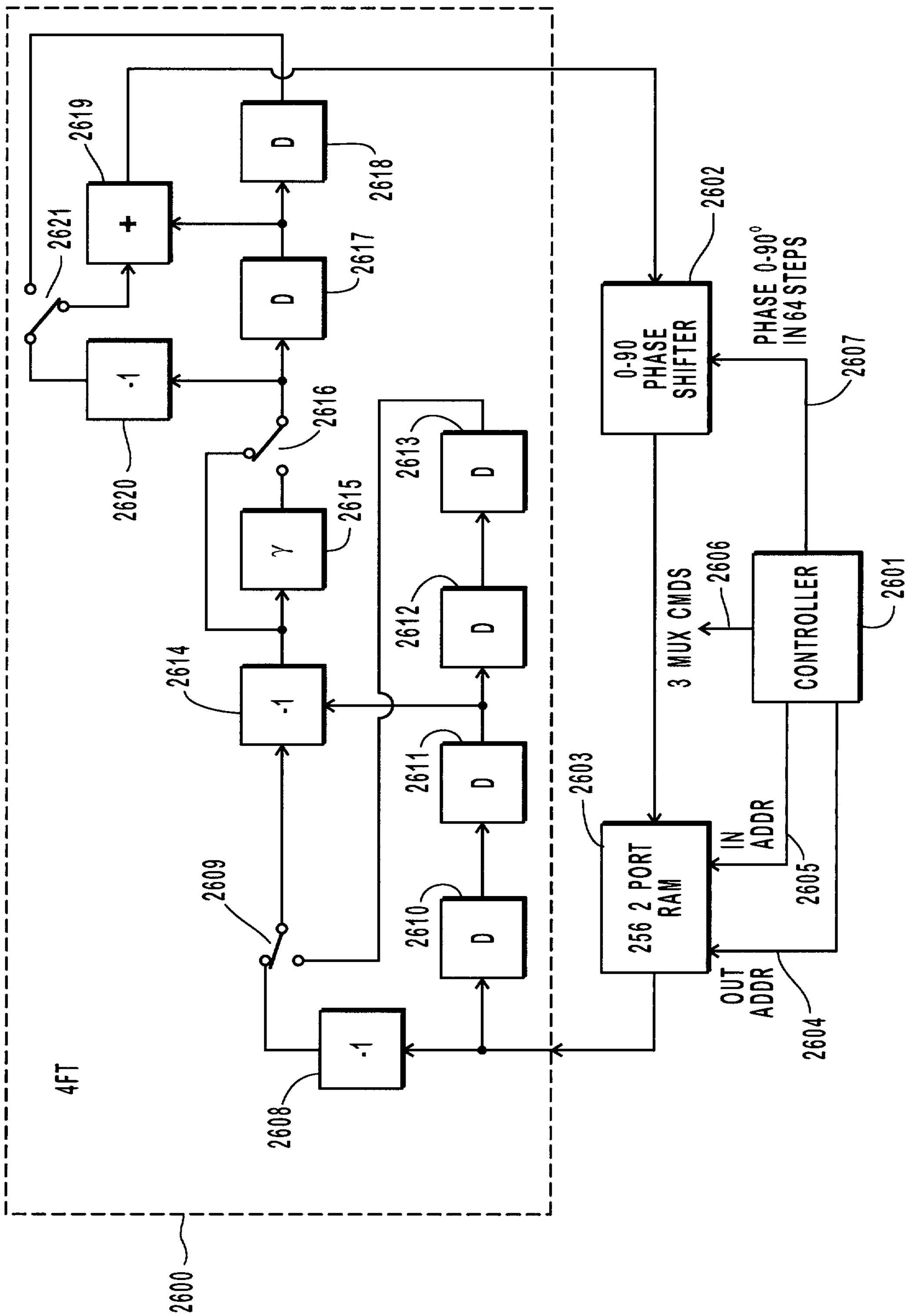

2500
XMIT DATA
ENCODER
2501
DOWN
SAMPLED
FIR
XMP
RCV
2502
2503
INPUT
BUFFER
2504
2505
2506
4FT
2507
THRESHOLD
DETECT
2508
TIMING
2509
÷ 2
CONJ
2512
2513
÷ 2
ROUND
2515
ØGEN
2516
OUTPUT
BUFFER
2517
CONJ
TO UPSAMPLE
XMT FIR
2518
2510
FFT RAM
XMIT BIT
2514
PHASE
SHIFTER
XTM BIT
2523
COMPLEX
TO ANGLE
2519
2511
BLOCK
SCALE
2520
SOFT
DATA
BUFFER
2522
TO RCV DECODER
2521
FRAME
SYNC

FIG. 25



4FT
2600
2601
CONTROLLER
2602
0-90 PHASE SHIFTER
2603
256 2 PORT RAM
2604
OUT ADDR
2605
IN ADDR
2606
3 MUX CMDS
2607
PHASE 0-90° IN 64 STEPS
2608
-1
2609
2610
D
2611
D
2612
D
2613
D
2614
-1
2615
γ
2616
2617
D
2618
D
2619
+
2620
-1
2621

FIG. 26

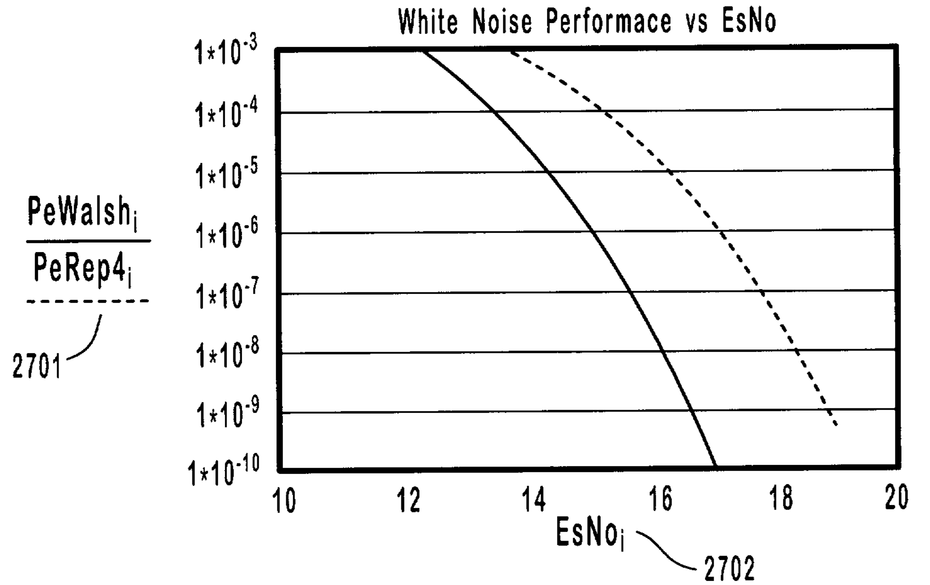


FIG. 27a

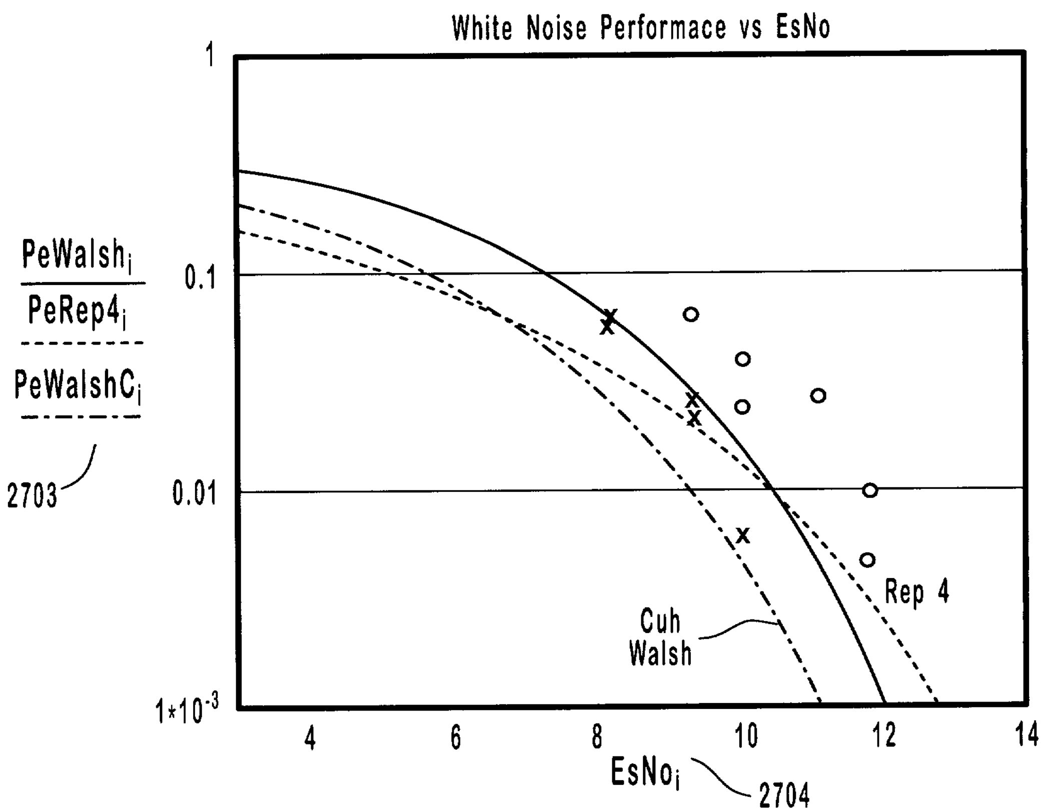


FIG. 27b

```
% finds likelihood of 16ary symbol error for nbe erasures
tr={1 –1; 1 1]; tr=[tr –tr; tr tr]; tr=[tr –tr; tr tr]; tr=[tr –tr; tr tr];
v=zeros(1,16);
nsym=zeros(1,16);
while sum(v)<16;
        [a,n]=max (tr*v');
        if n<16;
                nbe=sum(v= =0);
                nsym(nbe)=nsym(nbe) +1;
        end;
        k=1;
        v(k)= -(v(k)-1); % -1 or 0 – erasures
        while v(k)= =0;
                k=k+1;
                v(k)= -(v(k)-1); % -1 or 0 – erasures
        end;
end;
pe=.005:.005:.5;
for k=1:100;
        we(k)=sum(pe(k).^(1:16).*(1-pe(k)).^(15:-1:0).*nsym);
end;
rhe=1-((1-pe).^4+4*pe.*(1-pe).^3).^4; % repeat sym hard error
rea=1-(1-pe.^4).64; % repeat sym erasure error
plot (pe,we,pe,rea)
```

FIG. 28

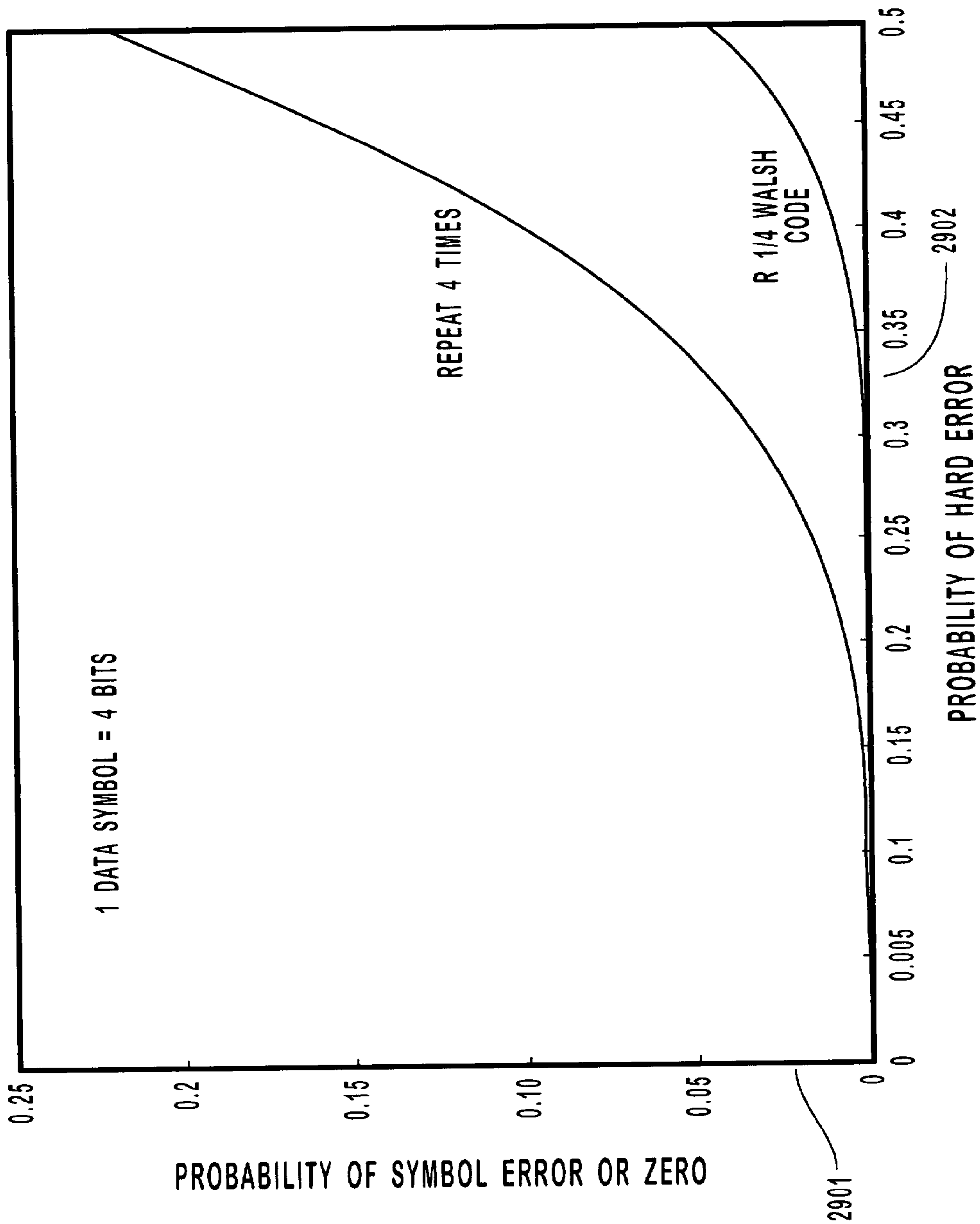

1 DATA SYMBOL = 4 BITS
REPEAT 4 TIMES
R 1/4 WALSH CODE
2901
2902
0
0.05
0.10
0.15
0.2
0.25
PROBABILITY OF SYMBOL ERROR OR ZERO
0
0.005
0.1
0.15
0.2
0.25
0.3
0.35
0.4
0.45
0.5
PROBABILITY OF HARD ERROR

FIG. 29

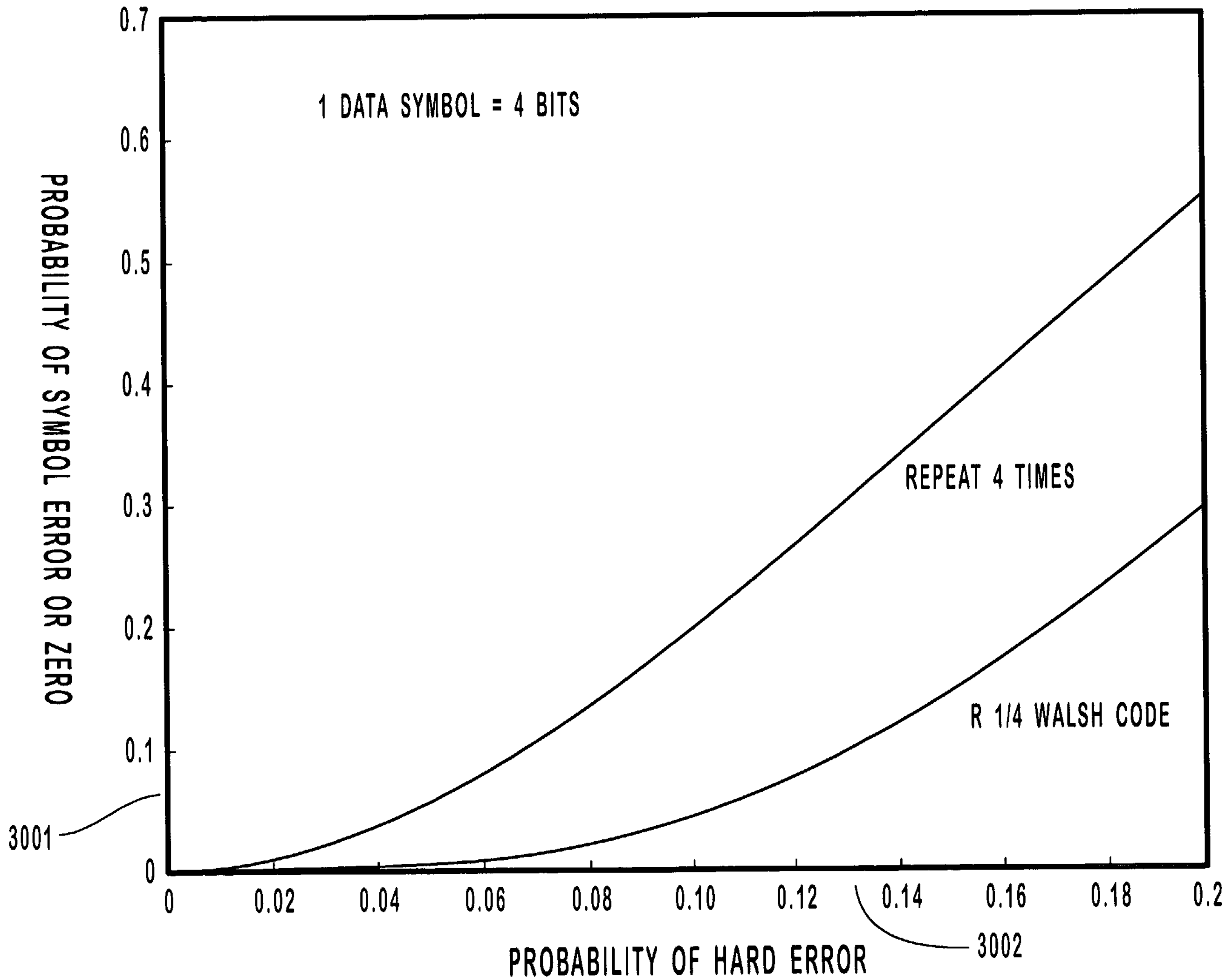

1 DATA SYMBOL = 4 BITS
REPEAT 4 TIMES
R 1/4 WALSH CODE
PROBABILITY OF SYMBOL ERROR OR ZERO
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
3001
0
0.02
0.04
0.06
0.08
0.10
0.12
0.14
0.16
0.18
0.2
3002
PROBABILITY OF HARD ERROR

FIG. 30

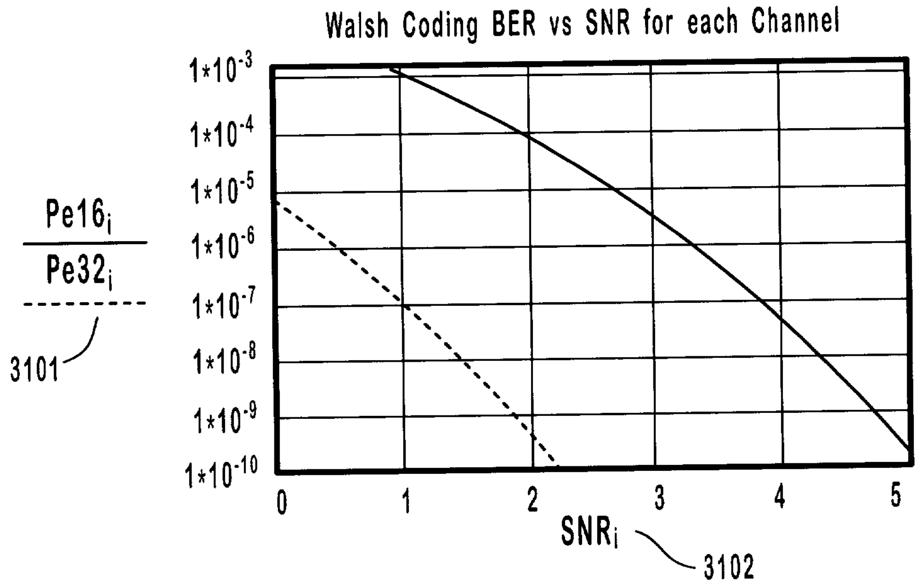

Walsh Coding BER vs SNR for each Channel
1*10^-3
1*10^-4
1*10^-5
1*10^-6
1*10^-7
1*10^-8
1*10^-9
1*10^-10
Pe16i
Pe32i
3101
0
1
2
3
4
5
SNRi
3102

FIG. 31

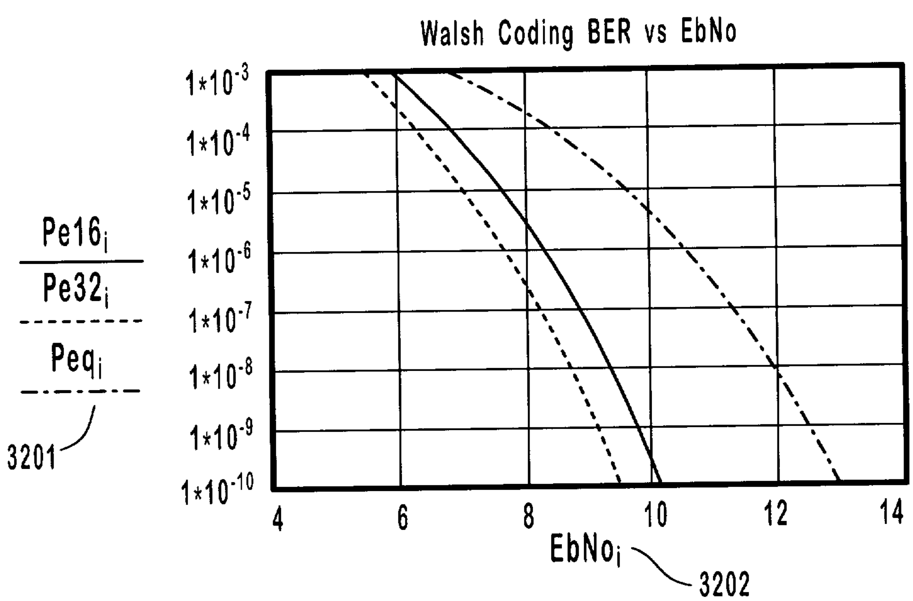

Walsh Coding BER vs EbNo
1*10^-3
1*10^-4
1*10^-5
1*10^-6
1*10^-7
1*10^-8
1*10^-9
1*10^-10
Pe16i
Pe32i
Peqi
3201
4
6
8
10
12
14
EbNoi
3202

FIG. 32

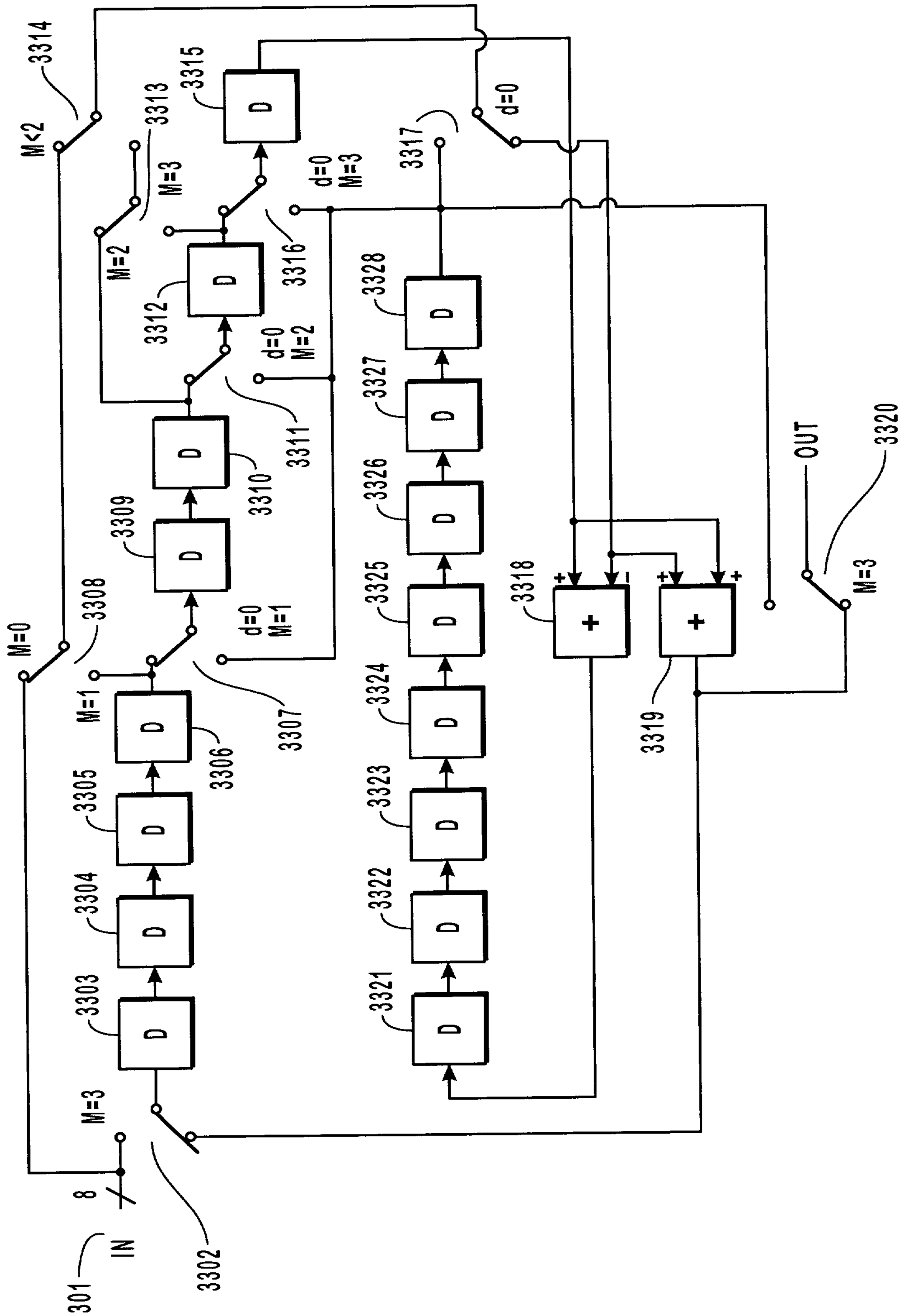

3301
IN
8
3302
M=3
M=0
3303
3304
3305
3306
M=1
3307
d=0
M=1
3308
3309
3310
3311
d=0
M=2
3312
M=2
M=3
3313
M<2
3314
3315
3316
d=0
M=3
3317
d=0
3318
3319
3320
OUT
M=3
3321
3322
3323
3324
3325
3326
3327
3328
D
+

FIG. 33

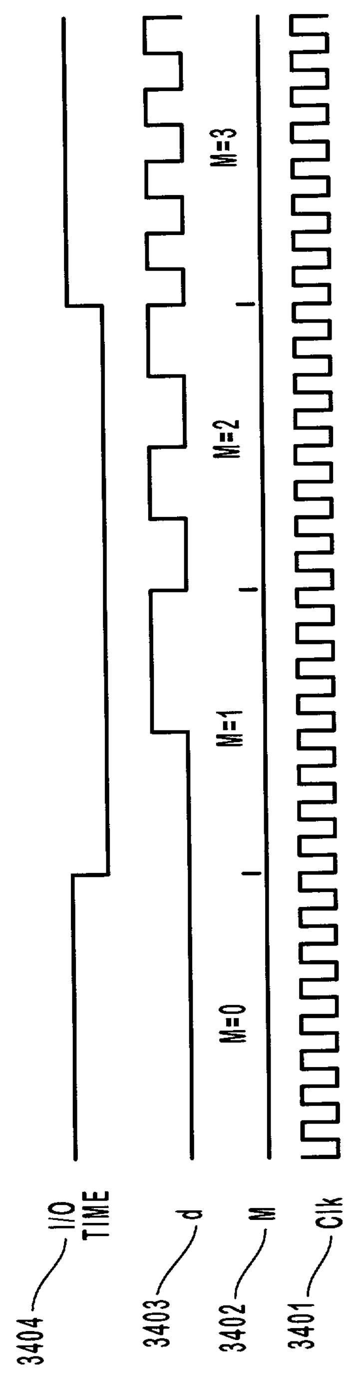


FIG. 34

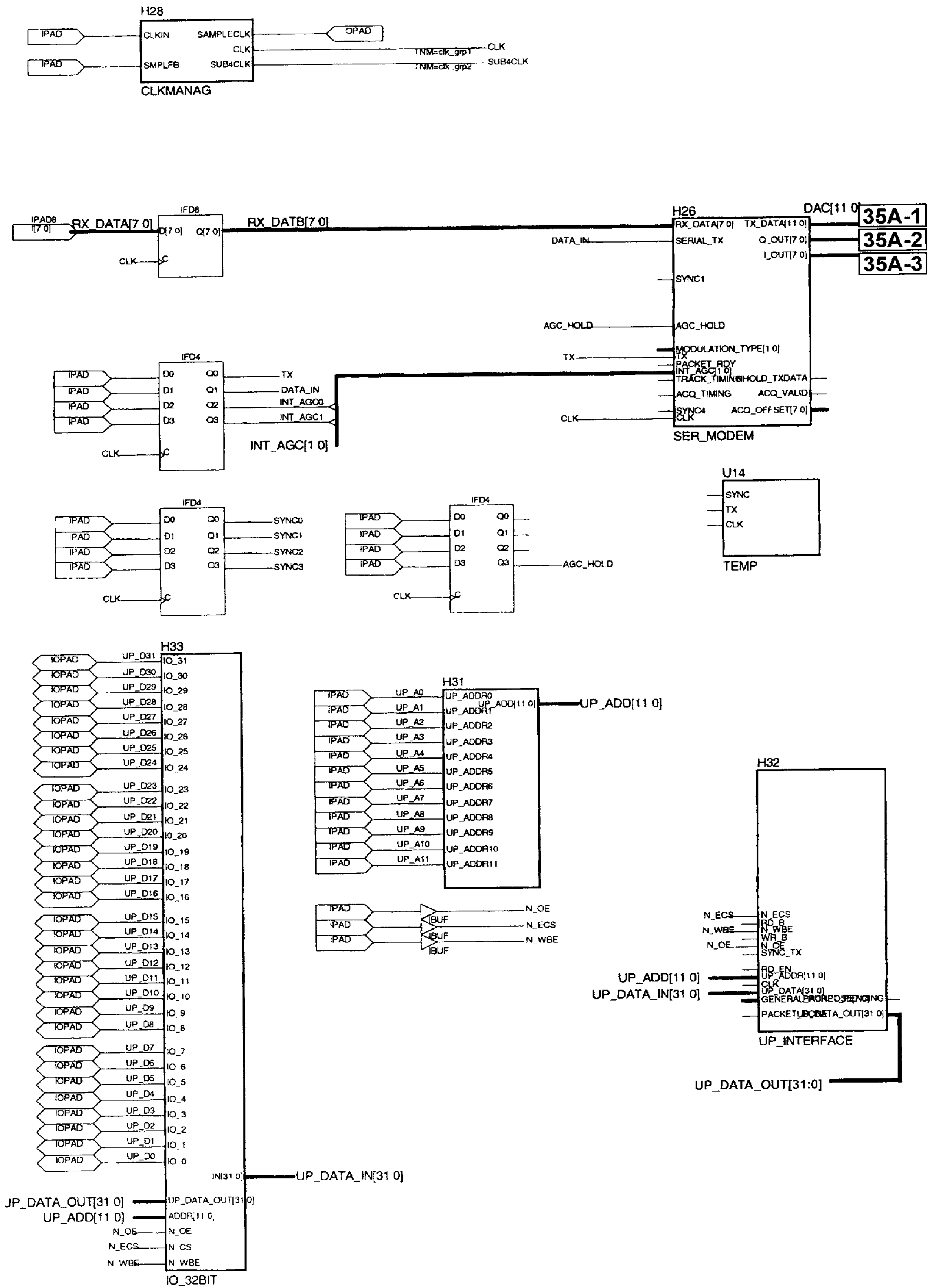
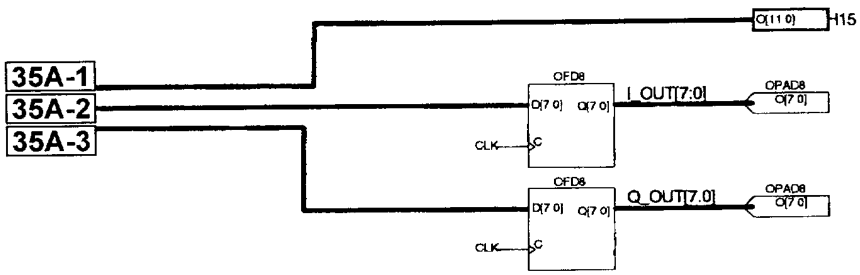
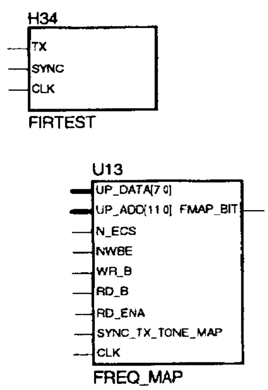

H28
IPAD
CLKIN
SAMPLECLK
OPAD
CLK
TNM=clk_grp1
CLK
IPAD
SMPLFB
SUB4CLK
TNM=clk_grp2
SUB4CLK
CLKMANAG
IPAD8
RX_DATA[7 0]
IFD8
D[7 0]
Q[7 0]
RX_DATB[7 0]
CLK
H26
DAC[11 0]
RX_DATA[7 0]
TX_DATA[11 0]
35A-1
DATA_IN
SERIAL_TX
Q_OUT[7 0]
35A-2
I_OUT[7 0]
35A-3
SYNC1
AGC_HOLD
AGC_HOLD
MODULATION_TYPE[1 0]
TX
TX
PACKET_RDY
INT_AGC[1 0]
TRACK_TIMING
HOLD_TXDATA
ACQ_TIMING
ACQ_VALID
SYNC4
ACQ_OFFSET[7 0]
CLK
CLK
SER_MODEM
IFD4
IPAD
D0
D1
D2
D3
Q0
Q1
Q2
Q3
TX
DATA_IN
INT_AGC0
INT_AGC1
INT_AGC[1 0]
U14
SYNC
TX
CLK
TEMP
SYNC0
SYNC1
SYNC2
SYNC3
AGC_HOLD
H33
IOPAD
UP_D31
IO_31
IO_0
IN[31 0]
UP_DATA_IN[31 0]
UP_DATA_OUT[31 0]
UP_DATA_OUT[31 0]
UP_ADD[11 0]
ADDR[11 0]
N_OE
N_ECS
N CS
N WBE
IO_32BIT
H31
UP_A0
UP_A11
UP_ADDR0
UP_ADDR11
UP_ADD[11 0]
UP_ADD[11 0]
IBUF
N_OE
N_ECS
N_WBE
H32
N_ECS
RD_B
N_WBE
WR_B
N_OE
SYNC_TX
RD_EN
UP_ADDR[11 0]
CLK
UP_DATA[31 0]
UP_ADD[11 0]
UP_DATA_IN[31 0]
PACKET
UP_DATA_OUT[31 0]
UP_INTERFACE
UP_DATA_OUT[31:0]

FIG. 35a-1


35A-1
35A-2
35A-3
O[11 0]
H15
OFD8
D[7 0]
Q[7 0]
C
CLK
I_OUT[7:0]
OPAD8
O[7 0]
OFD8
D[7 0]
Q[7 0]
C
CLK
Q_OUT[7:0]
OPAD8
O[7 0]


H34
TX
SYNC
CLK
FIRTEST
U13
UP_DATA[7 0]
UP_ADD[11 0]
FMAP_BIT
N_ECS
NWBE
WR_B
RD_B
RD_ENA
SYNC_TX_TONE_MAP
CLK
FREQ_MAP

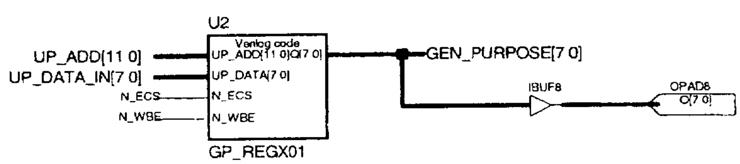
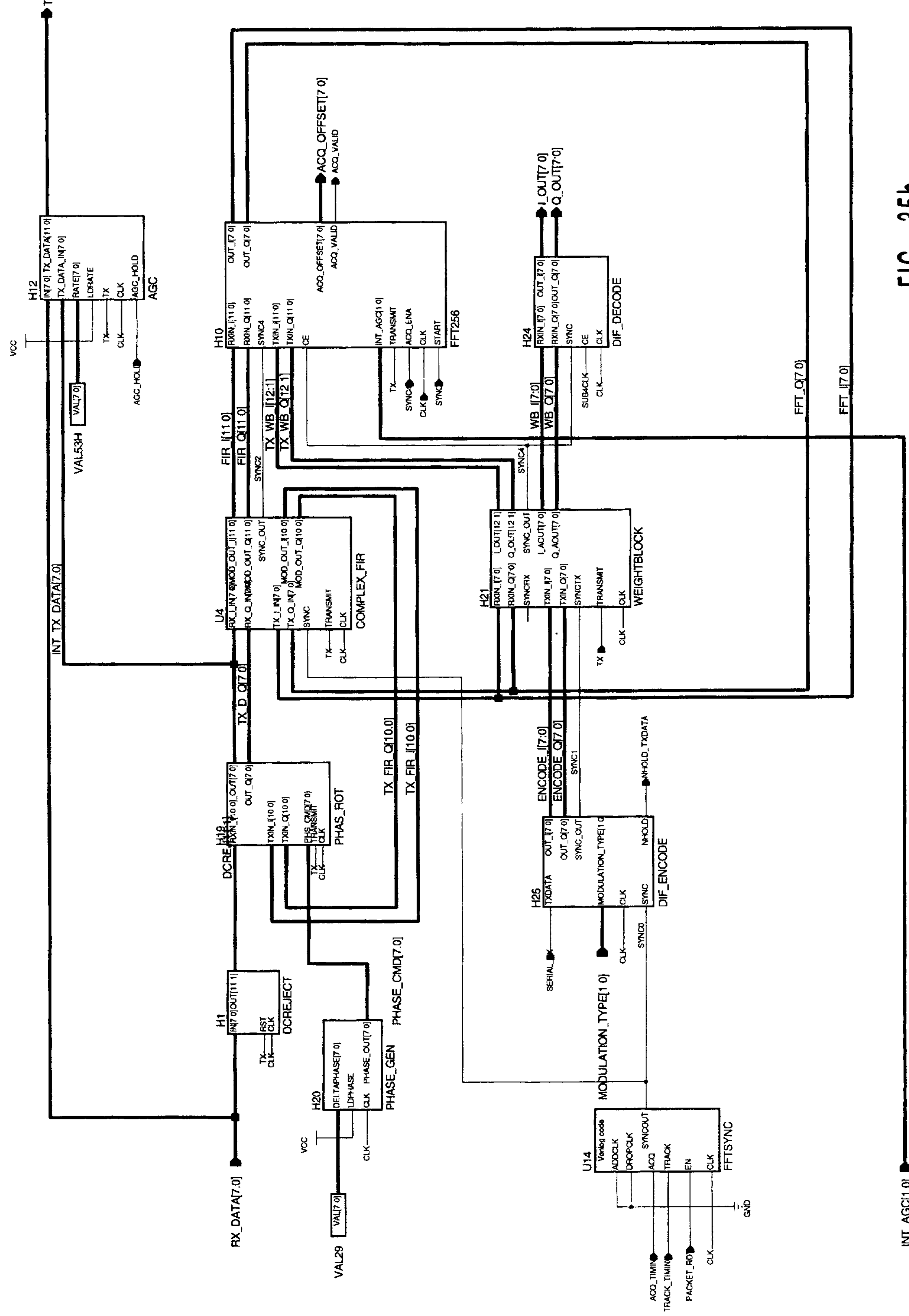

U2
Verilog code
UP_ADD[11 0]
UP_DATA_IN[7 0]
N_ECS
N_WBE
UP_ADD[11 0]
Q[7 0]
UP_DATA[7 0]
N_ECS
N_WBE
GP_REGX01
GEN_PURPOSE[7 0]
IBUF8
OPAD8
O[7 0]

FIG. 35a-2



TX_DATA[11:0]
AGC
FFT256
ACQ_OFFSET[7:0]
ACQ_VALID
I_OUT[7:0]
Q_OUT[7:0]
DIF_DECODE
COMPLEX_FIR
WEIGHTBLOCK
PHAS_ROT
DIF_ENCODE
DCREJECT
PHASE_GEN
PHASE_CMD[7:0]
MODULATION_TYPE[1:0]
FFTSYNC
RX_DATA[7:0]
INT_AGC[1:0]

FIG. 35b

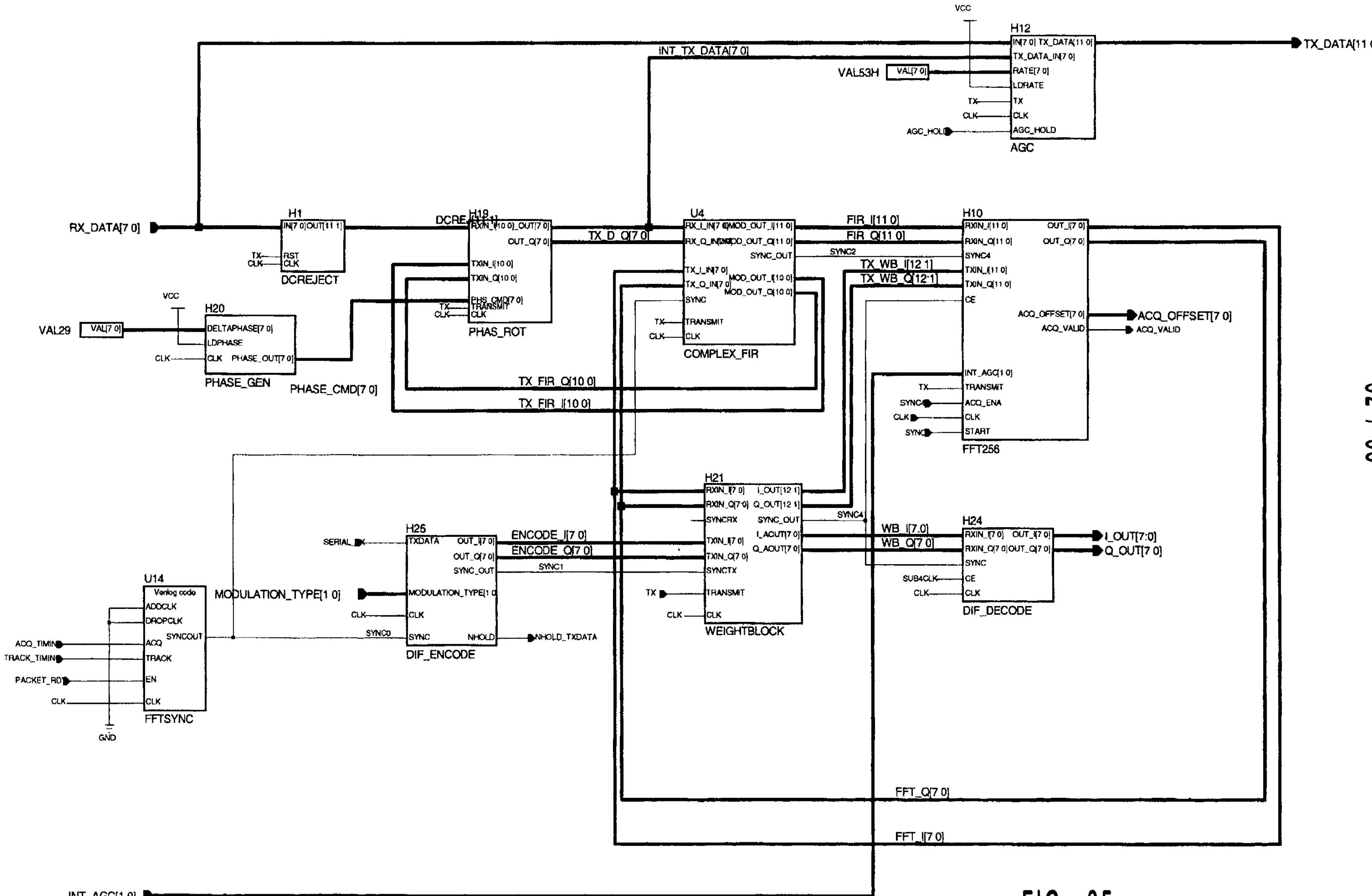

VCC
H12
TX_DATA[11 0]
INT_TX_DATA[7 0]
VAL53H
VAL[7 0]
AGC_HOLD
AGC
RX_DATA[7 0]
H1
DCREJECT
H19
PHAS_ROT
TX_D_Q[7 0]
U4
COMPLEX_FIR
FIR_I[11 0]
FIR_Q[11 0]
SYNC2
TX_WB_I[12 1]
TX_WB_Q[12 1]
H10
FFT256
ACQ_OFFSET[7 0]
ACQ_VALID
H20
VAL29
PHASE_GEN
PHASE_CMD[7 0]
TX_FIR_Q[10 0]
TX_FIR_I[10 0]
H21
WEIGHTBLOCK
SYNC4
WB_I[7 0]
WB_Q[7 0]
H24
DIF_DECODE
I_OUT[7:0]
Q_OUT[7 0]
H25
DIF_ENCODE
SERIAL
ENCODE_I[7 0]
ENCODE_Q[7 0]
SYNC1
MODULATION_TYPE[1 0]
NHOLD_TXDATA
U14
Verilog code
FFTSYNC
ACQ_TIMIN
TRACK_TIMIN
PACKET_RD
GND
FFT_Q[7 0]
FFT_I[7 0]
INT_AGC[1 0]

FIG. 35c

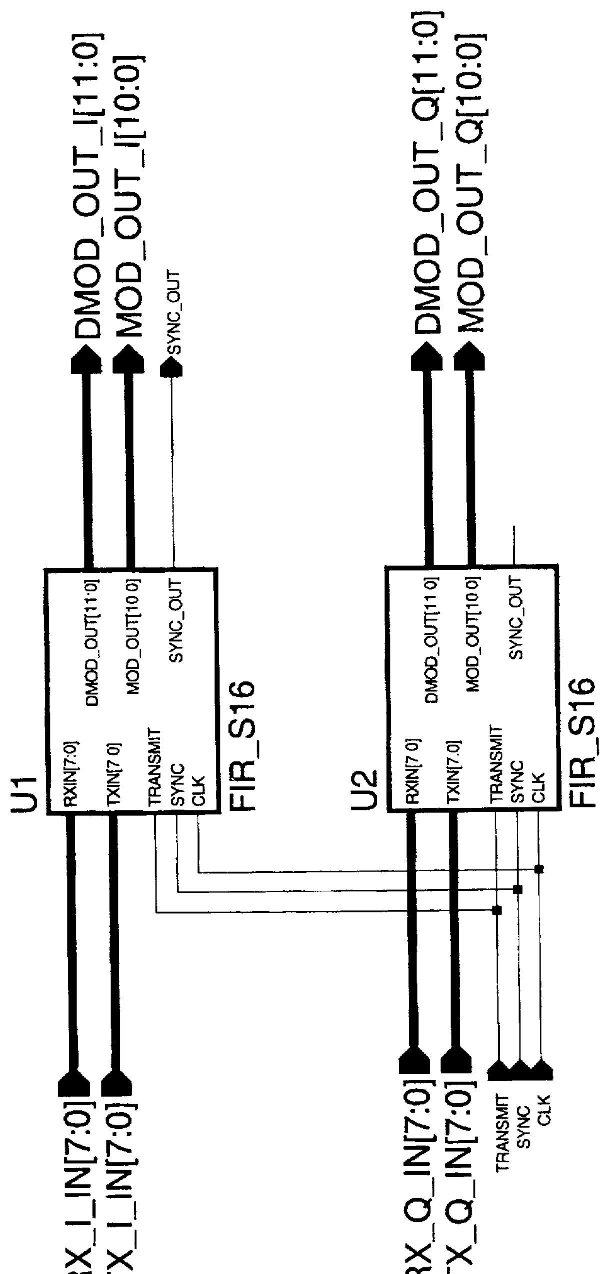
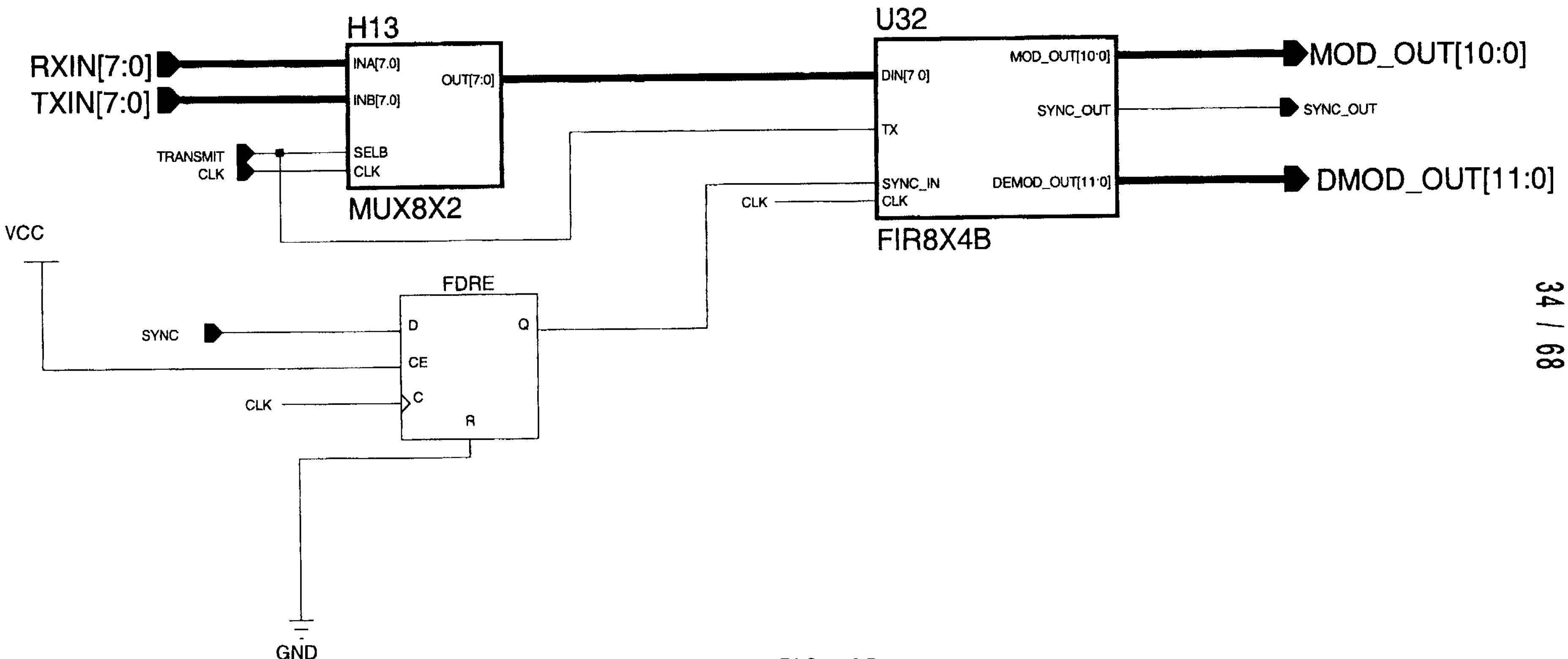

DMOD_OUT_I[11:0]
MOD_OUT_I[10:0]
SYNC_OUT
DMOD_OUT_Q[11:0]
MOD_OUT_Q[10:0]
U1
RXIN[7:0]
TXIN[7:0]
TRANSMIT
SYNC
CLK
DMOD_OUT[11:0]
MOD_OUT[10:0]
SYNC_OUT
FIR_S16
U2
RXIN[7:0]
TXIN[7:0]
TRANSMIT
SYNC
CLK
DMOD_OUT[11:0]
MOD_OUT[10:0]
SYNC_OUT
FIR_S16
RX_I_IN[7:0]
TX_I_IN[7:0]
RX_Q_IN[7:0]
TX_Q_IN[7:0]
TRANSMIT
SYNC
CLK

FIG. 35d



H13
RXIN[7:0]
TXIN[7:0]
INA[7:0]
INB[7:0]
OUT[7:0]
SELB
CLK
TRANSMIT
CLK
MUX8X2
U32
DIN[7:0]
TX
SYNC_IN
CLK
MOD_OUT[10:0]
SYNC_OUT
DEMOD_OUT[11:0]
FIR8X4B
MOD_OUT[10:0]
SYNC_OUT
DMOD_OUT[11:0]
CLK
VCC
FDRE
D
CE
C
R
Q
SYNC
CLK
GND

FIG. 35e

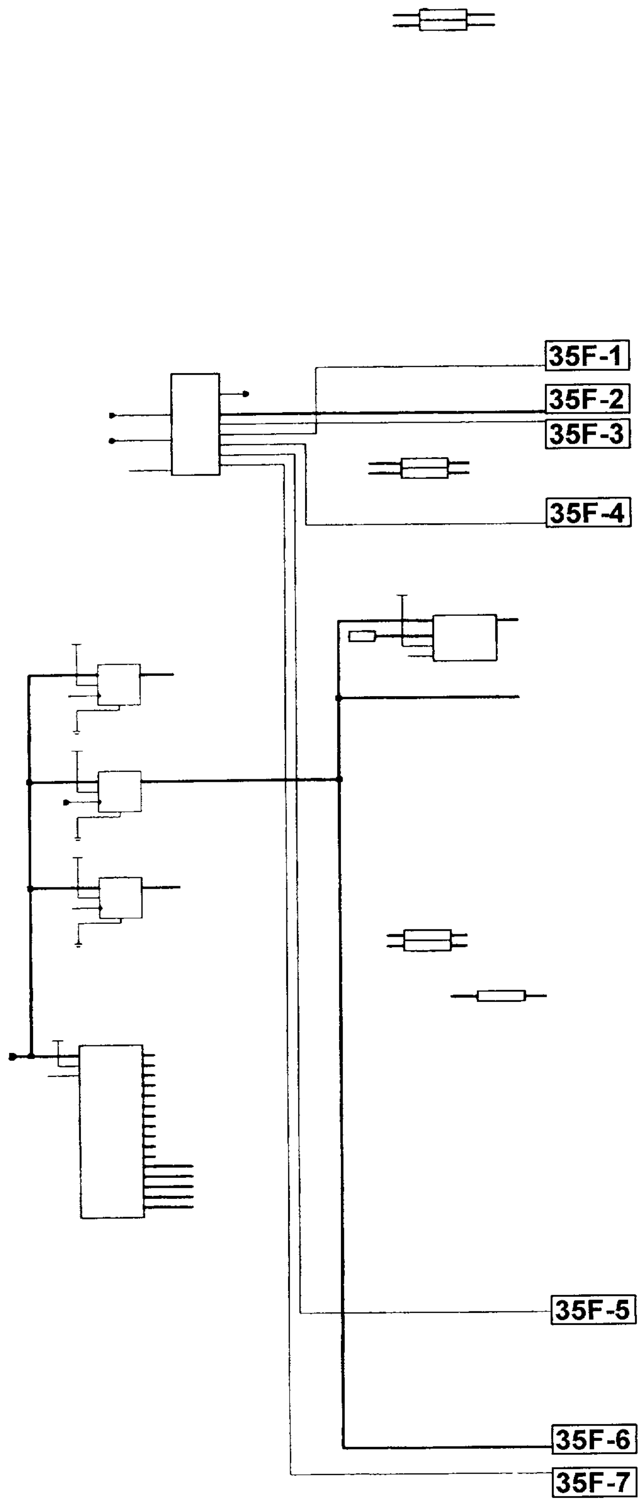


FIG. 35f-1

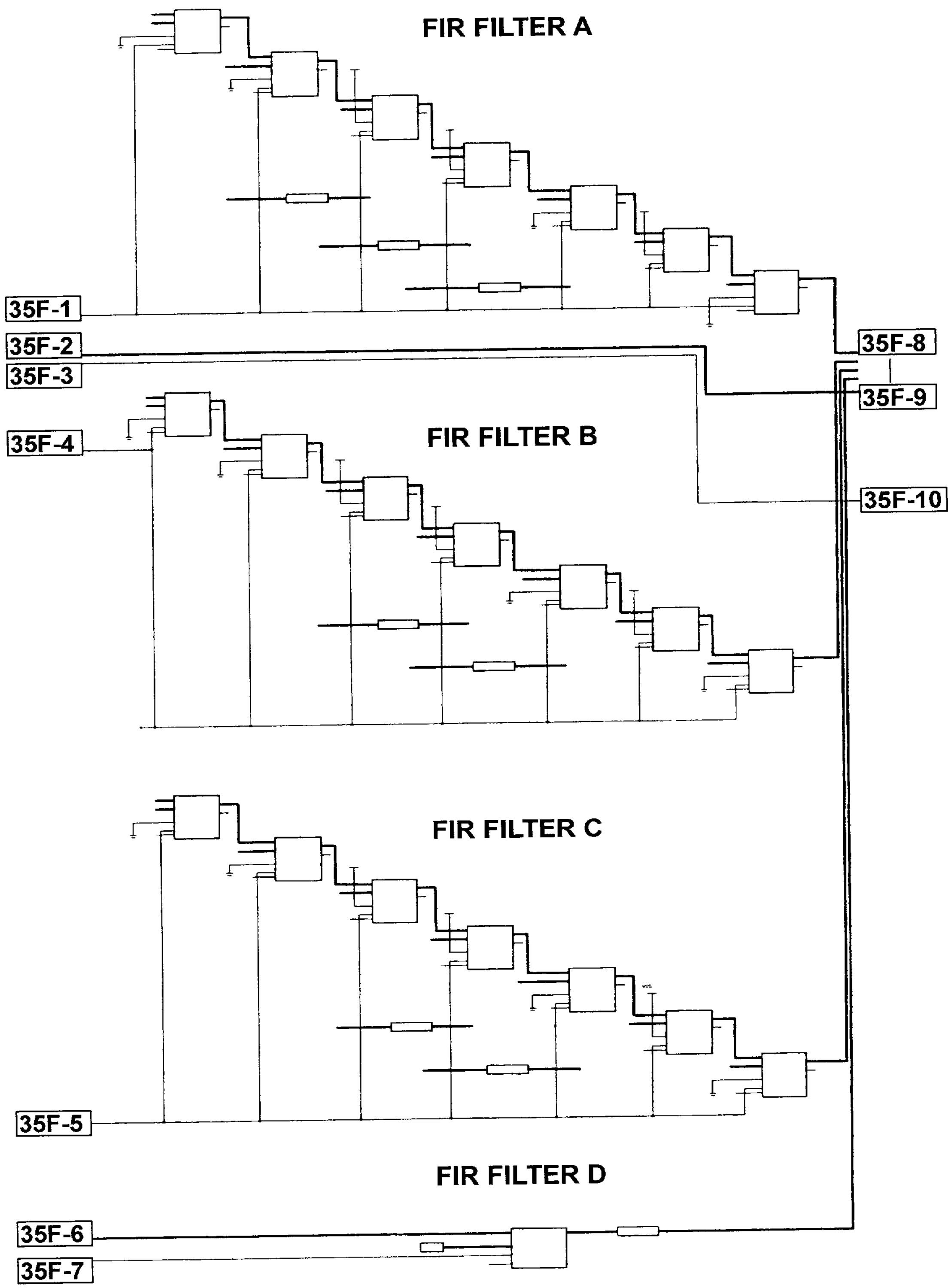

FIR FILTER A
FIR FILTER B
FIR FILTER C
FIR FILTER D
35F-1
35F-2
35F-3
35F-4
35F-5
35F-6
35F-7
35F-8
35F-9
35F-10

FIG. 35f-2

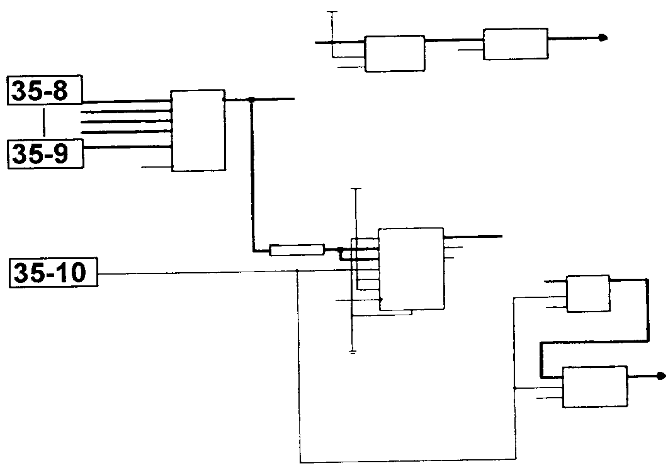


FIG. 35f-3

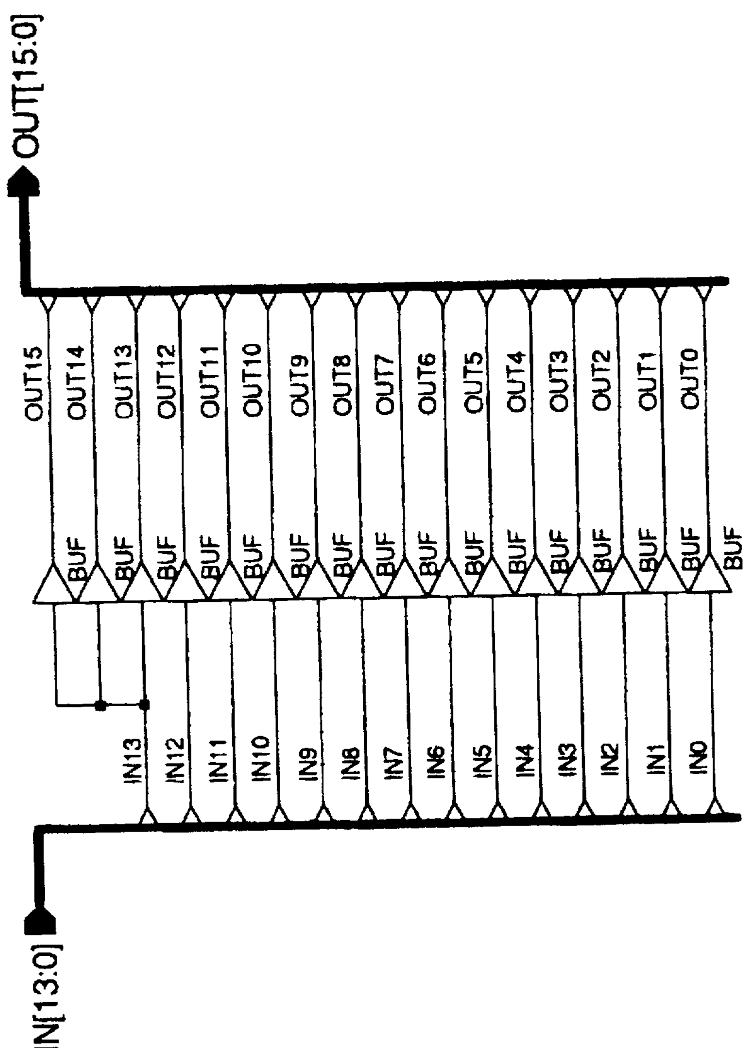

OUT[15:0]
IN[13:0]
OUT15
OUT14
OUT13
OUT12
OUT11
OUT10
OUT9
OUT8
OUT7
OUT6
OUT5
OUT4
OUT3
OUT2
OUT1
OUT0
BUF
IN13
IN12
IN11
IN10
IN9
IN8
IN7
IN6
IN5
IN4
IN3
IN2
IN1
IN0

FIG. 35g

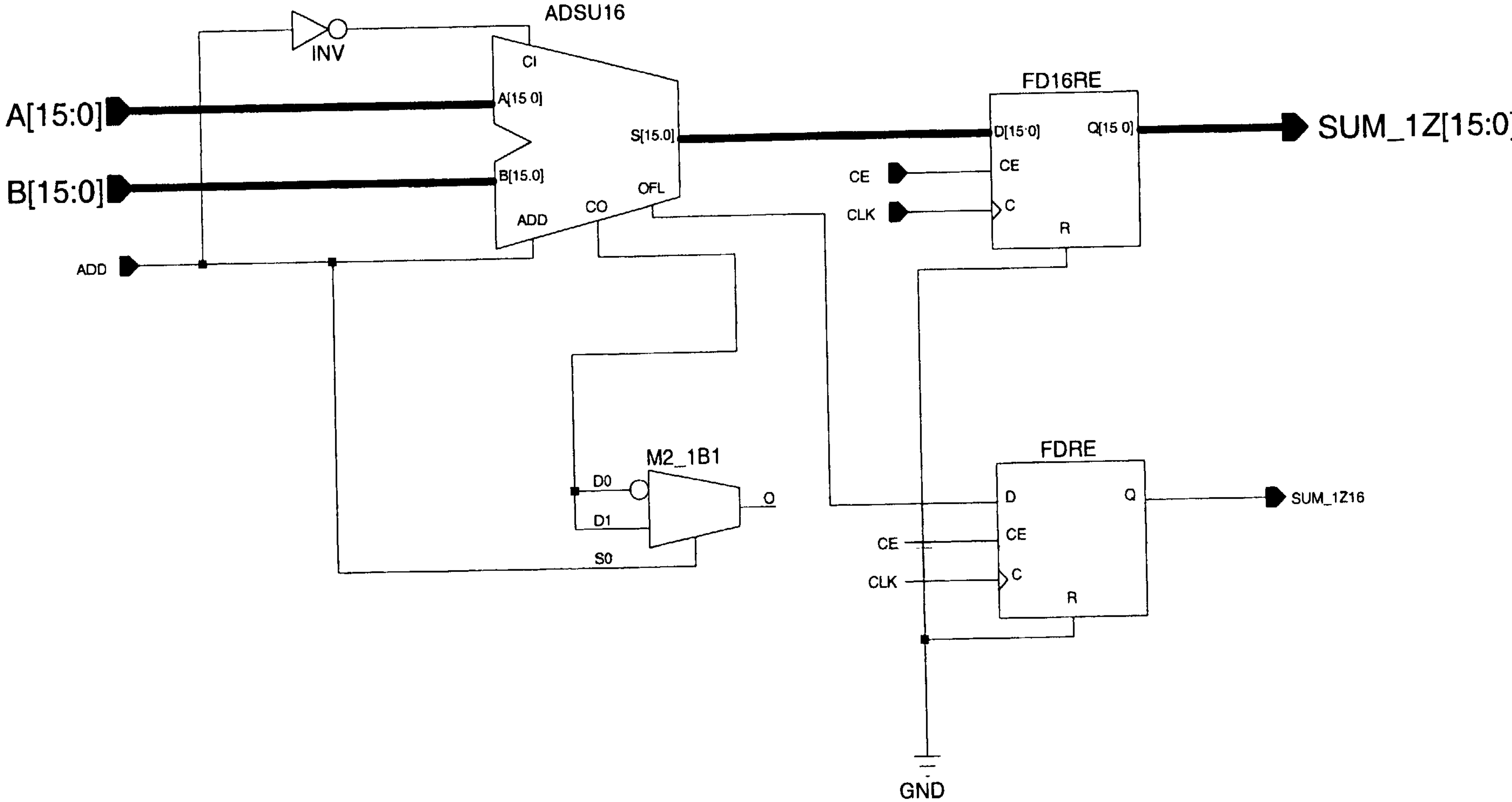

ADSU16
INV
CI
A[15:0]
A[15 0]
B[15:0]
B[15.0]
ADD
ADD
CO
OFL
S[15.0]
FD16RE
D[15:0]
Q[15 0]
SUM_1Z[15:0]
CE
CE
CLK
C
R
M2_1B1
D0
D1
S0
O
FDRE
D
Q
SUM_1Z16
CE
CE
CLK
C
R
GND

FIG. 35h

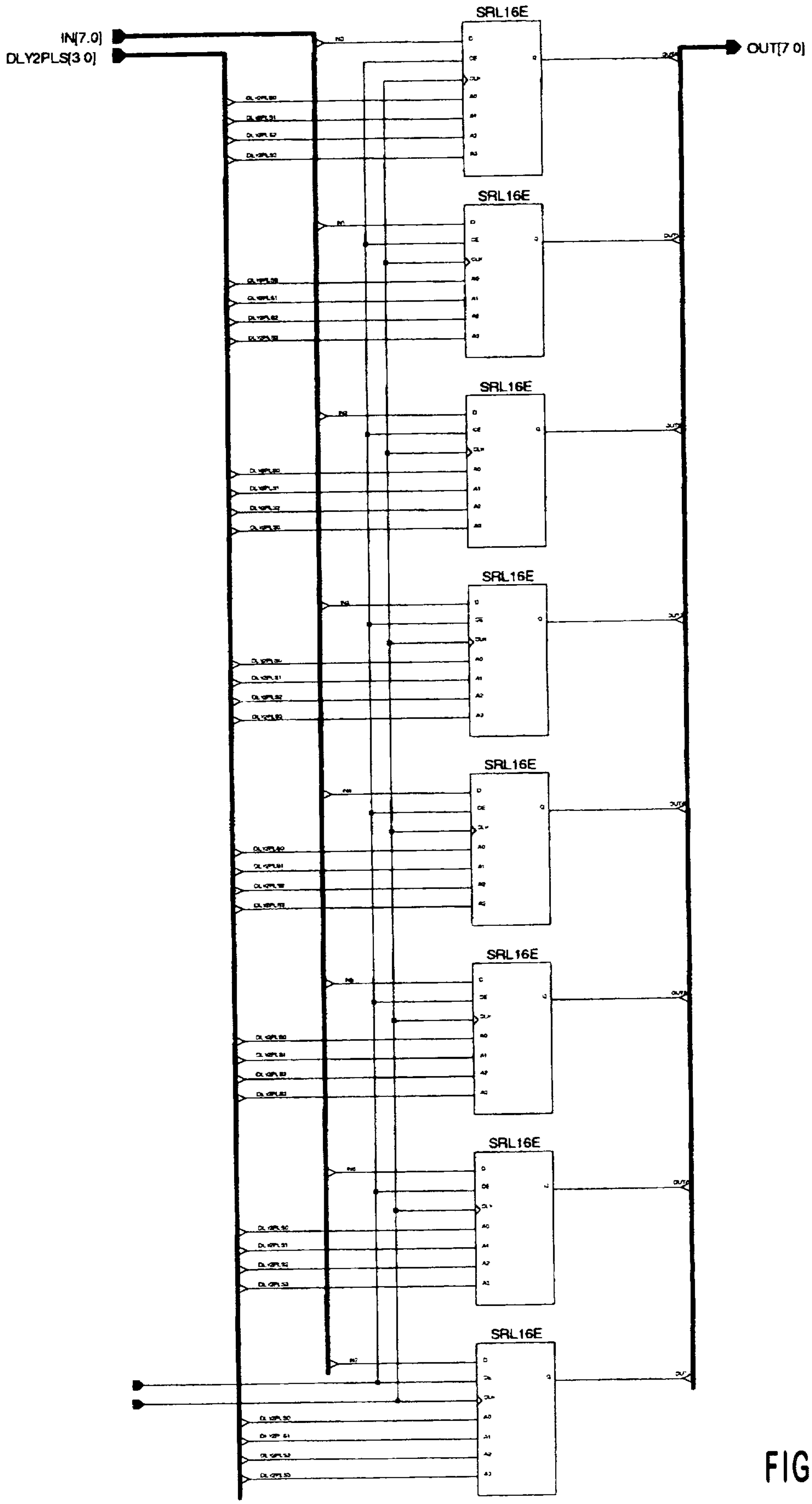

IN[7:0]
DLY2PLS[3:0]
OUT[7:0]
SRL16E
SRL16E
SRL16E
SRL16E
SRL16E
SRL16E
SRL16E
SRL16E

FIG. 35i

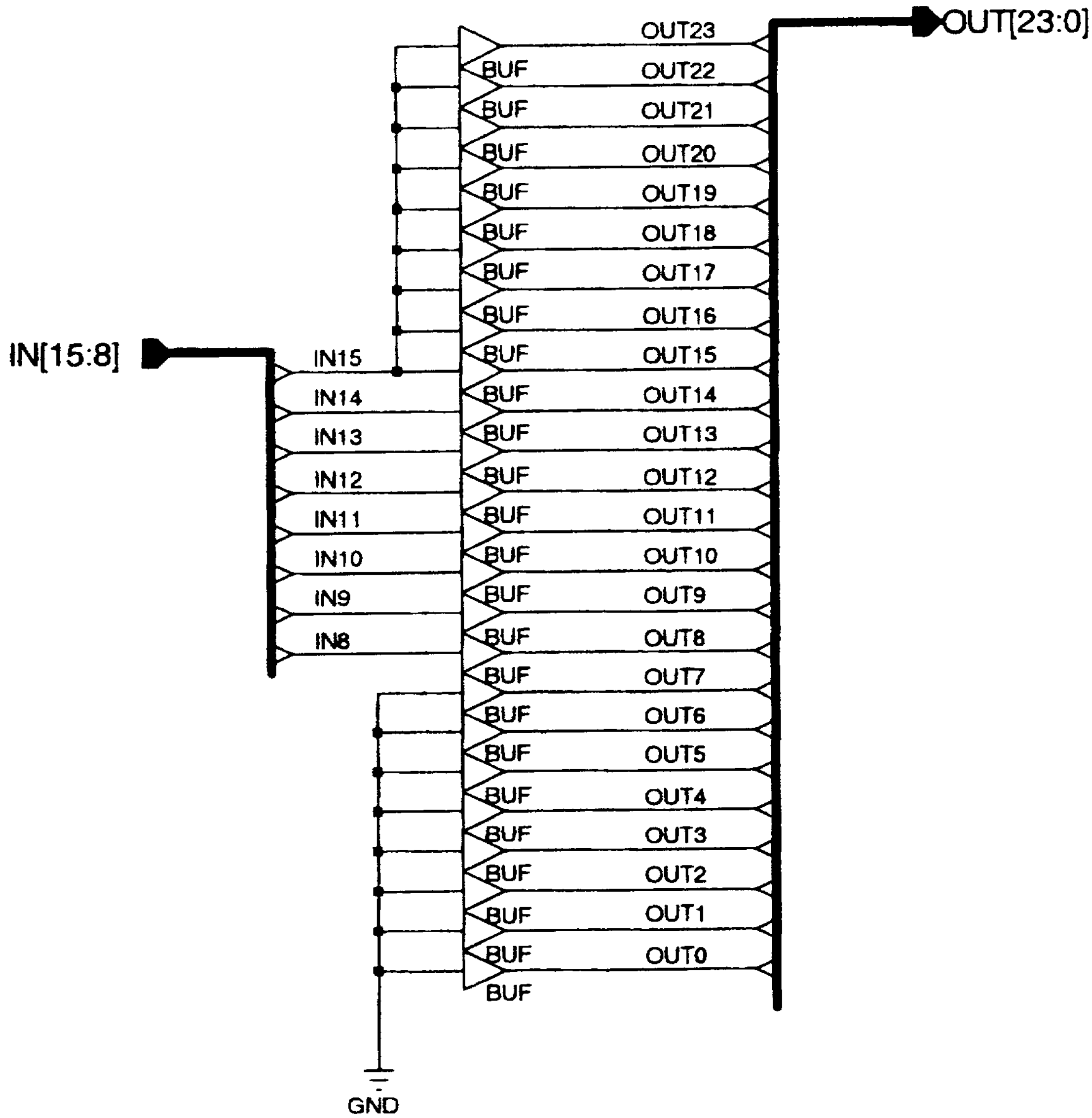

OUT[23:0]
IN[15:8]
OUT23
OUT22
OUT21
OUT20
OUT19
OUT18
OUT17
OUT16
OUT15
OUT14
OUT13
OUT12
OUT11
OUT10
OUT9
OUT8
OUT7
OUT6
OUT5
OUT4
OUT3
OUT2
OUT1
OUT0
IN15
IN14
IN13
IN12
IN11
IN10
IN9
IN8
BUF
GND

FIG. 35j

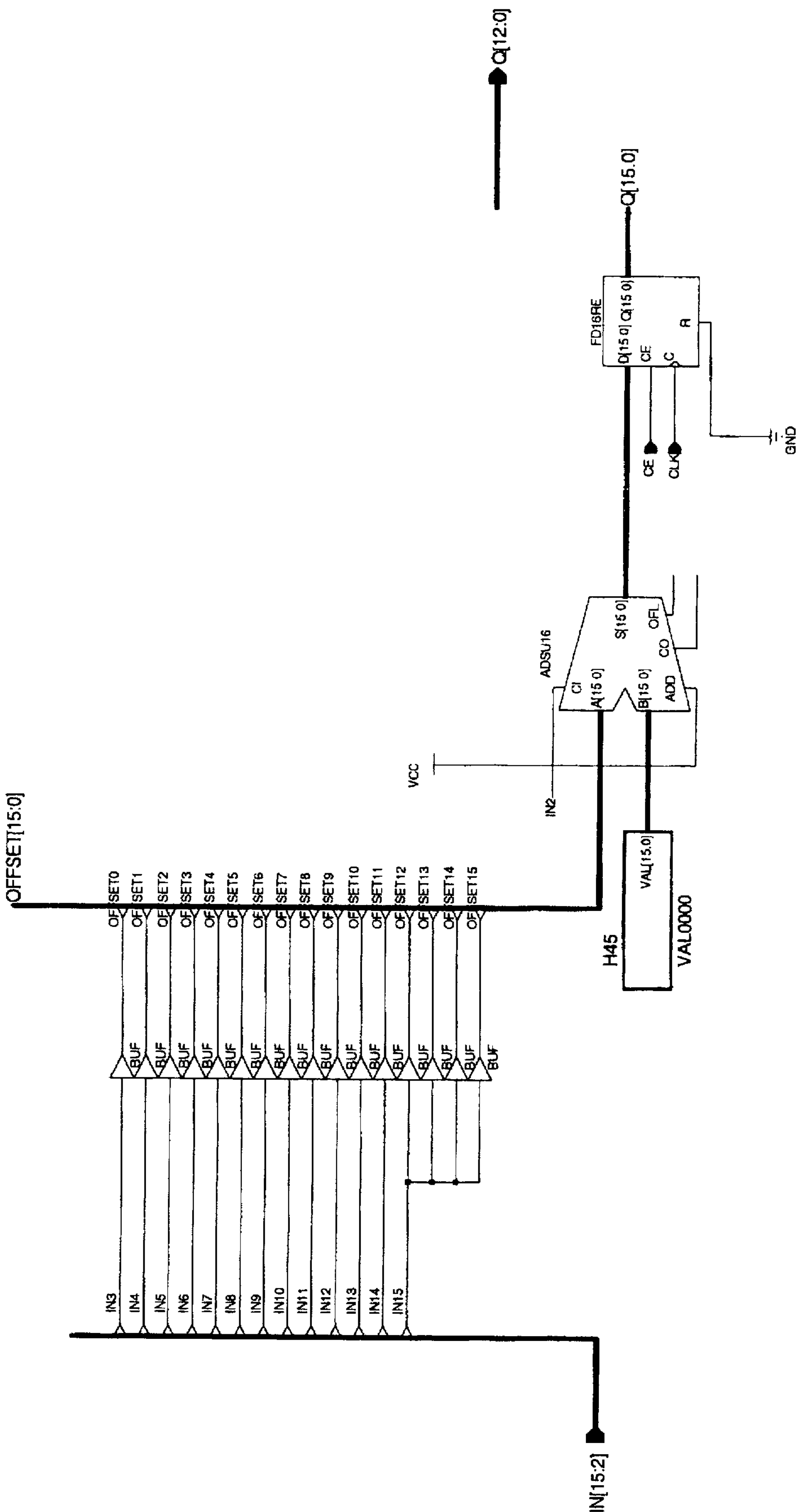

Q[12:0]
Q[15:0]
FD16RE
D[15:0]
Q[15:0]
CE
C
R
GND
CE
CLK
ADSU16
CI
A[15:0]
B[15:0]
ADD
S[15:0]
OFL
CO
VCC
IN2
OFFSET[15:0]
OFFSET0
OFFSET1
OFFSET2
OFFSET3
OFFSET4
OFFSET5
OFFSET6
OFFSET7
OFFSET8
OFFSET9
OFFSET10
OFFSET11
OFFSET12
OFFSET13
OFFSET14
OFFSET15
BUF
H45
VAL[15:0]
VAL0000
IN3
IN4
IN5
IN6
IN7
IN8
IN9
IN10
IN11
IN12
IN13
IN14
IN15
IN[15:2]

FIG. 35k

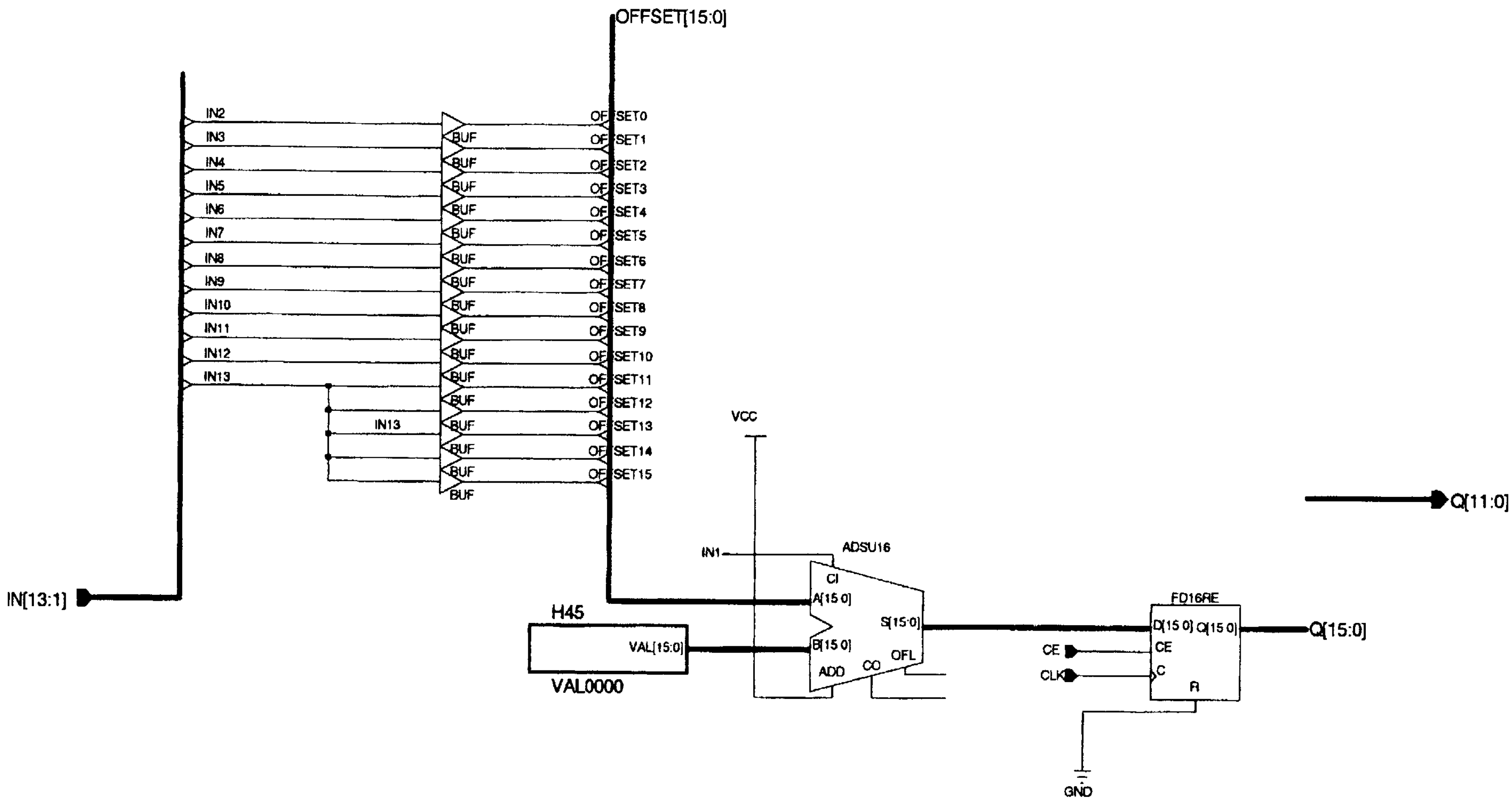

OFFSET[15:0]
IN2
IN3
IN4
IN5
IN6
IN7
IN8
IN9
IN10
IN11
IN12
IN13
IN13
BUF
OFFSET0
OFFSET1
OFFSET2
OFFSET3
OFFSET4
OFFSET5
OFFSET6
OFFSET7
OFFSET8
OFFSET9
OFFSET10
OFFSET11
OFFSET12
OFFSET13
OFFSET14
OFFSET15
IN[13:1]
VCC
IN1
ADSU16
CI
A[15:0]
B[15:0]
ADD
CO
OFL
S[15:0]
H45
VAL[15:0]
VAL0000
FD16RE
D[15:0]
Q[15:0]
CE
C
R
CE
CLK
GND
Q[15:0]
Q[11:0]

FIG. 35I

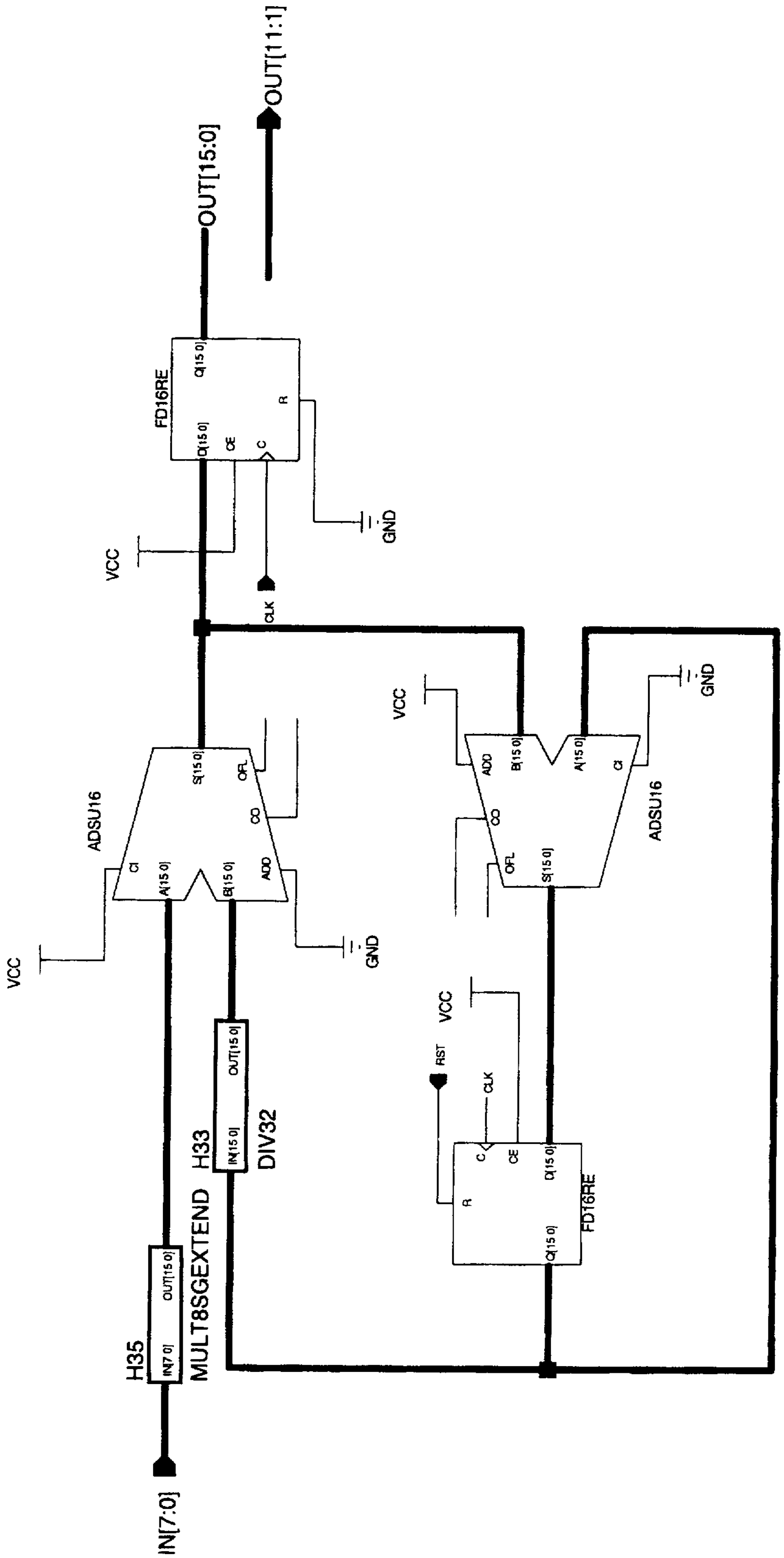

OUT[15:0]
OUT[11:1]
FD16RE
VCC
GND
CLK
ADSU16
VCC
GND
ADSU16
VCC
GND
VCC
RST
CLK
FD16RE
H33
DIV32
H35
MULT8SGEXTEND
IN[7:0]

FIG. 35m

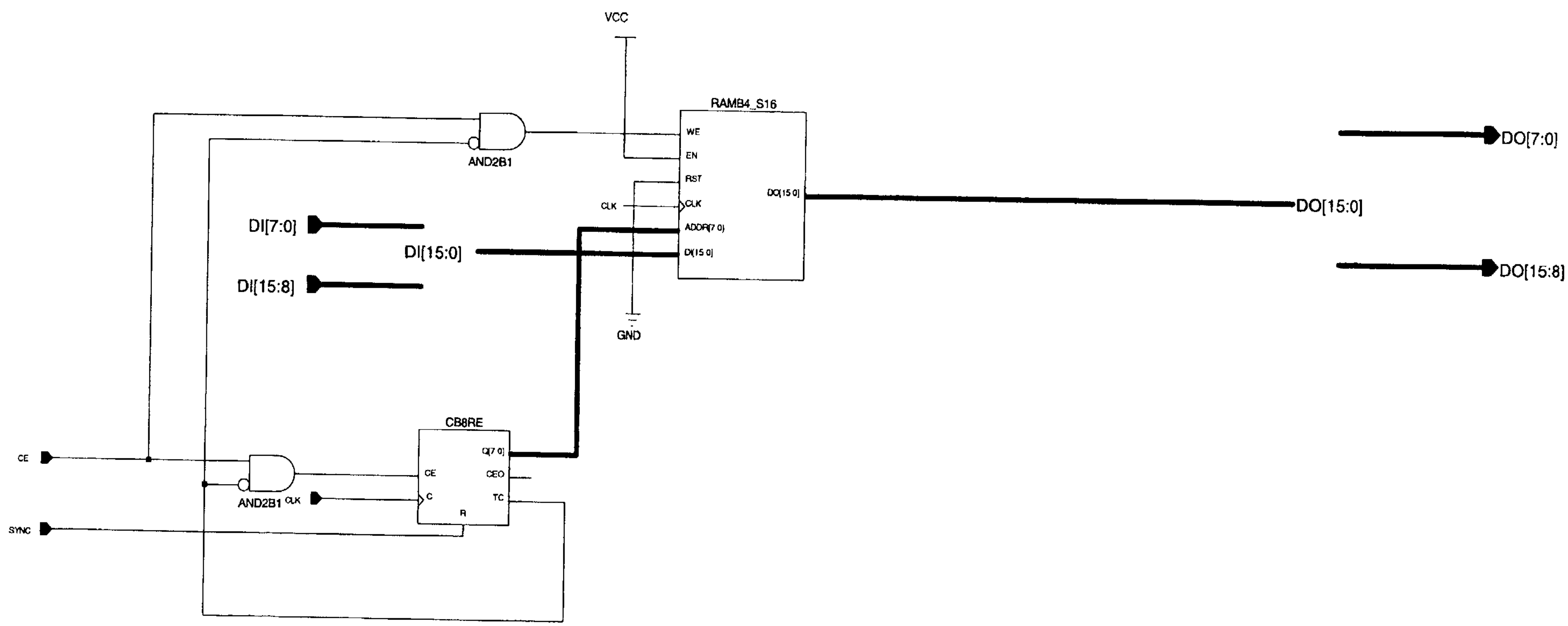

VCC
RAMB4_S16
WE
EN
RST
CLK
ADDR[7:0]
DI[15:0]
DO[15:0]
CLK
GND
AND2B1
DI[7:0]
DI[15:0]
DI[15:8]
DO[7:0]
DO[15:0]
DO[15:8]
CB8RE
Q[7:0]
CE
CEO
C
TC
R
AND2B1
CLK
CE
SYNC

FIG. 35n

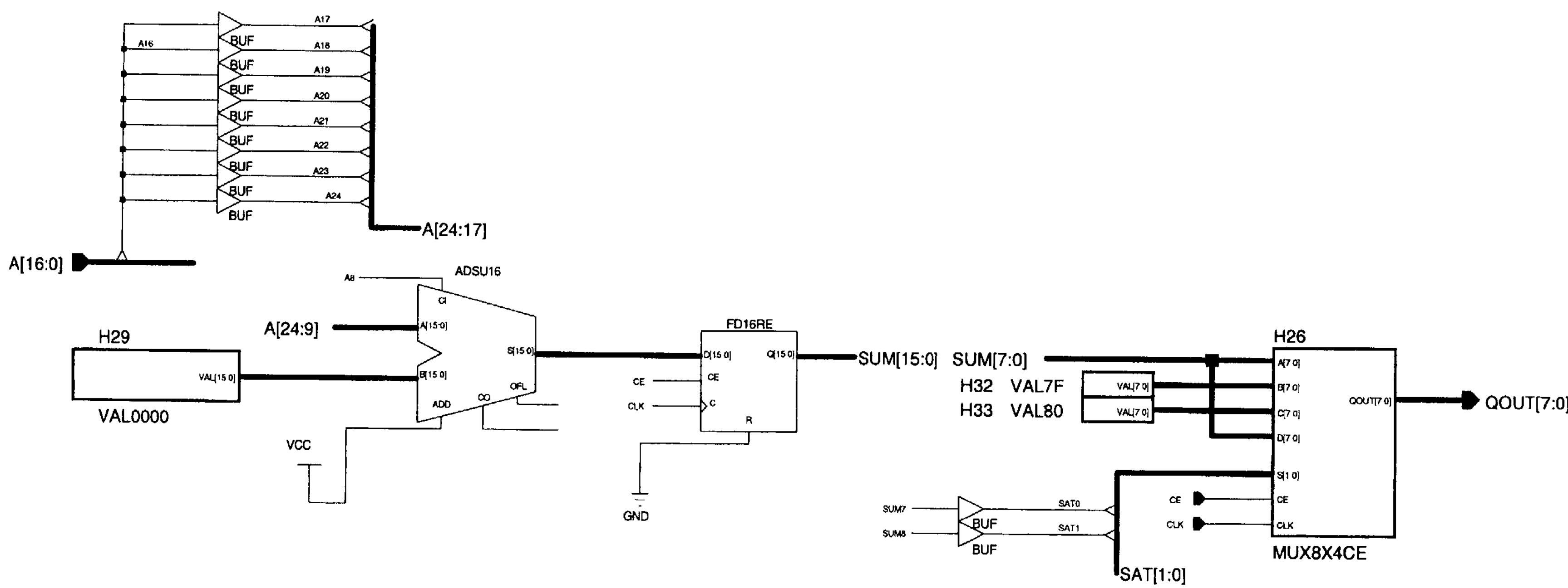

A[16:0]
A16
A17
A18
A19
A20
A21
A22
A23
A24
BUF
BUF
BUF
BUF
BUF
BUF
BUF
BUF
A[24:17]
ADSU16
A8
CI
A[15:0]
B[15:0]
ADD
CO
OFL
S[15:0]
A[24:9]
H29
VAL[15:0]
VAL0000
VCC
FD16RE
D[15:0]
CE
C
R
Q[15:0]
CE
CLK
GND
SUM[15:0]
SUM[7:0]
H32 VAL7F
H33 VAL80
VAL[7:0]
VAL[7:0]
H26
A[7:0]
B[7:0]
C[7:0]
D[7:0]
S[1:0]
CE
CLK
QOUT[7:0]
MUX8X4CE
QOUT[7:0]
SUM7
SUM8
BUF
BUF
SAT0
SAT1
SAT[1:0]
CE
CLK

FIG. 35o

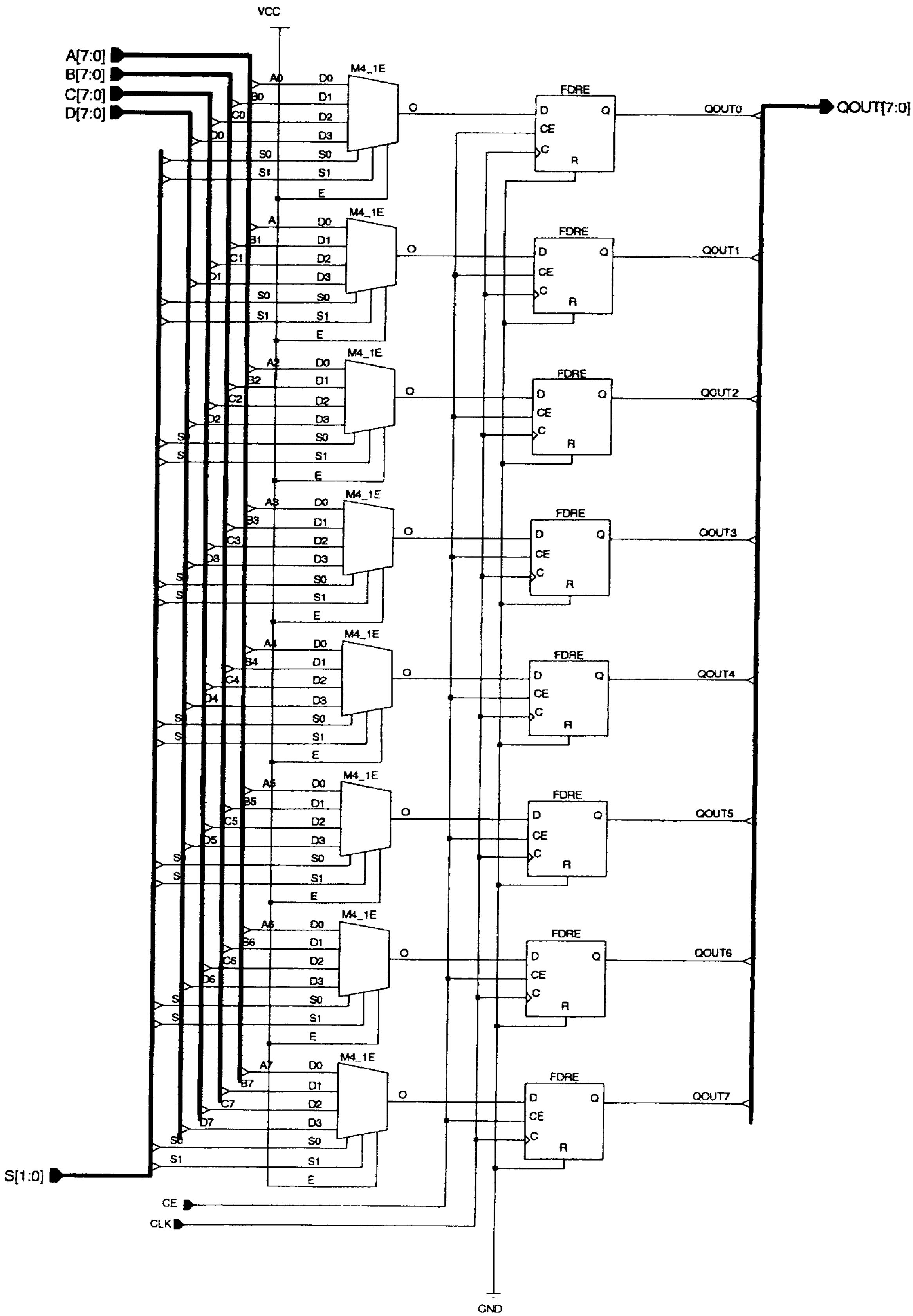

VCC
A[7:0]
B[7:0]
C[7:0]
D[7:0]
M4_1E
D0
D1
D2
D3
S0
S1
E
O
FDRE
D
Q
CE
C
R
QOUT0
QOUT1
QOUT2
QOUT3
QOUT4
QOUT5
QOUT6
QOUT7
QOUT[7:0]
S[1:0]
CE
CLK
GND

FIG. 35p

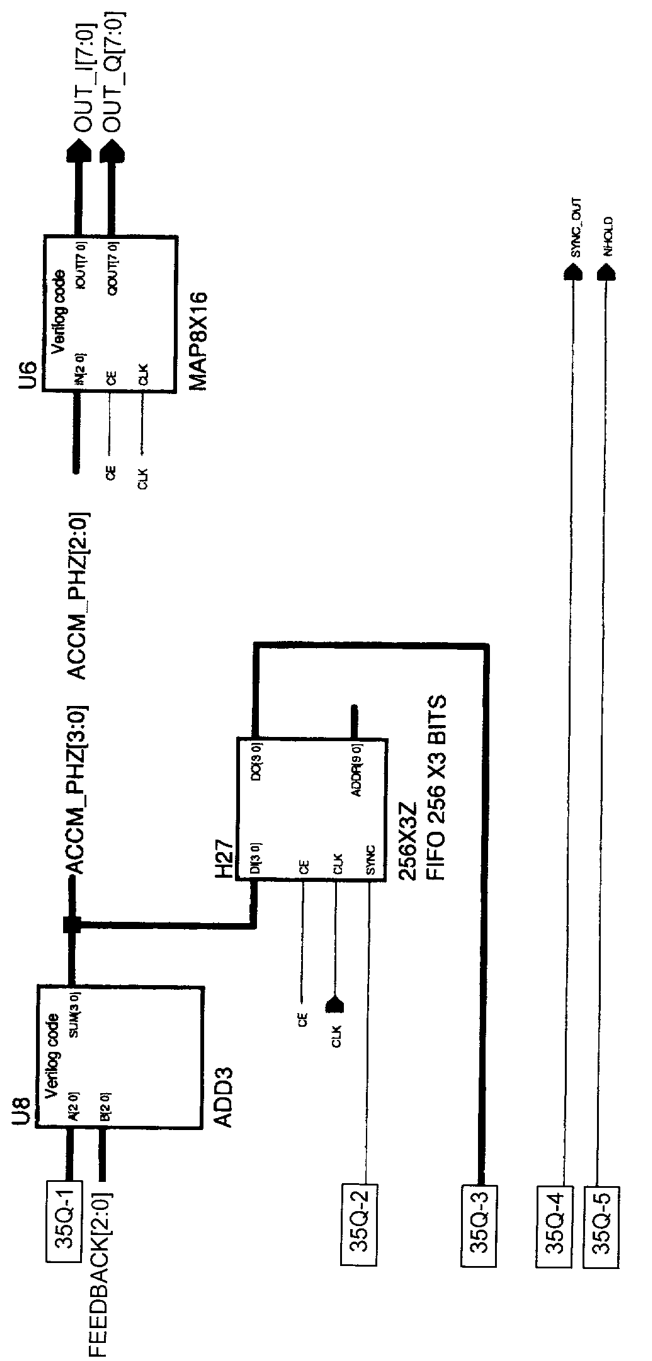
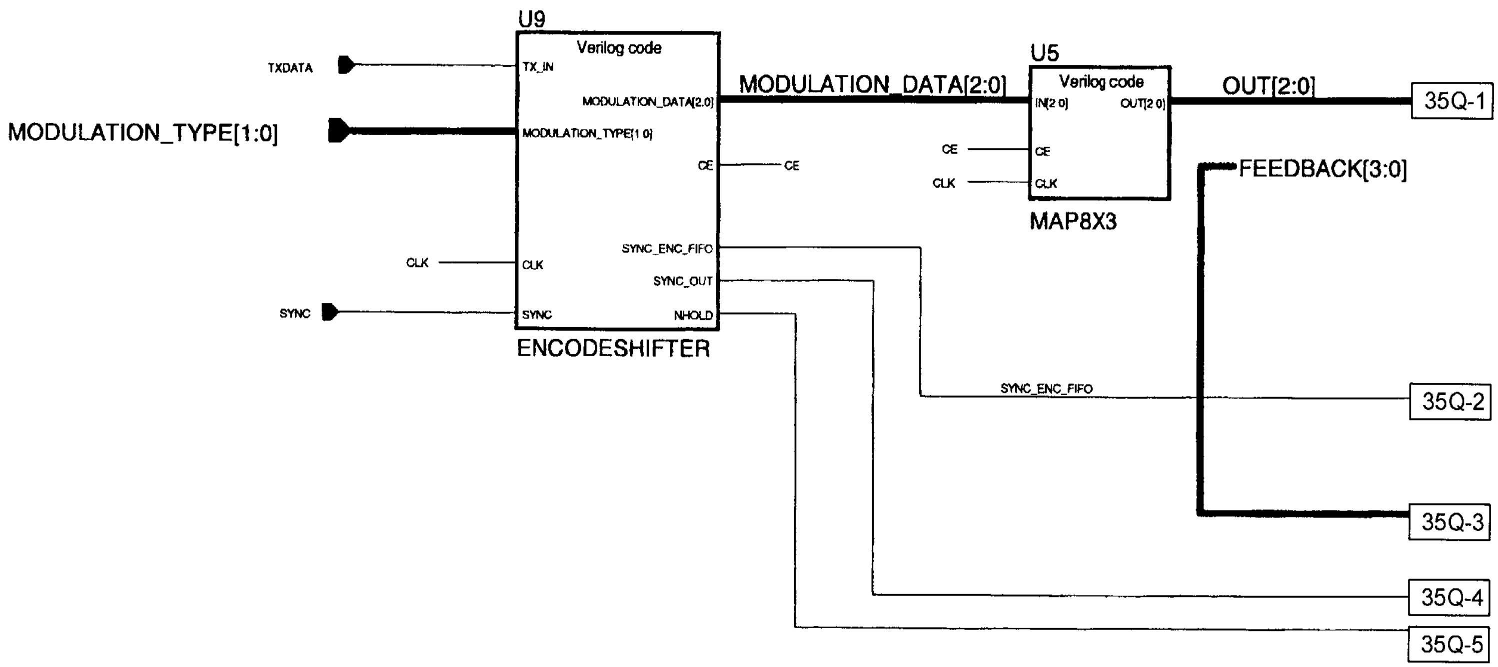

OUT_I[7:0]
OUT_Q[7:0]
U6
Verilog code
IN[2:0]
CE
CLK
IOUT[7:0]
QOUT[7:0]
MAP8X16
CE
CLK
SYNC_OUT
NHOLD
ACCM_PHZ[3:0]
ACCM_PHZ[2:0]
H27
DI[3:0]
CE
CLK
SYNC
DO[3:0]
ADDR[9:0]
256X3Z
FIFO 256 X3 BITS
U8
Verilog code
A[2:0]
B[2:0]
SUM[3:0]
ADD3
CE
CLK
35Q-1
FEEDBACK[2:0]
35Q-2
35Q-3
35Q-4
35Q-5

FIG. 35q-2



U9
Verilog code
TXDATA
TX_IN
MODULATION_TYPE[1:0]
MODULATION_TYPE[1:0]
MODULATION_DATA[2:0]
CE
CE
CLK
CLK
SYNC
SYNC
SYNC_ENC_FIFO
SYNC_OUT
NHOLD
ENCODESHIFTER
MODULATION_DATA[2:0]
U5
Verilog code
IN[2:0]
OUT[2:0]
CE
CE
CLK
CLK
MAP8X3
OUT[2:0]
FEEDBACK[3:0]
SYNC_ENC_FIFO
35Q-1
35Q-2
35Q-3
35Q-4
35Q-5

FIG. 35q-1

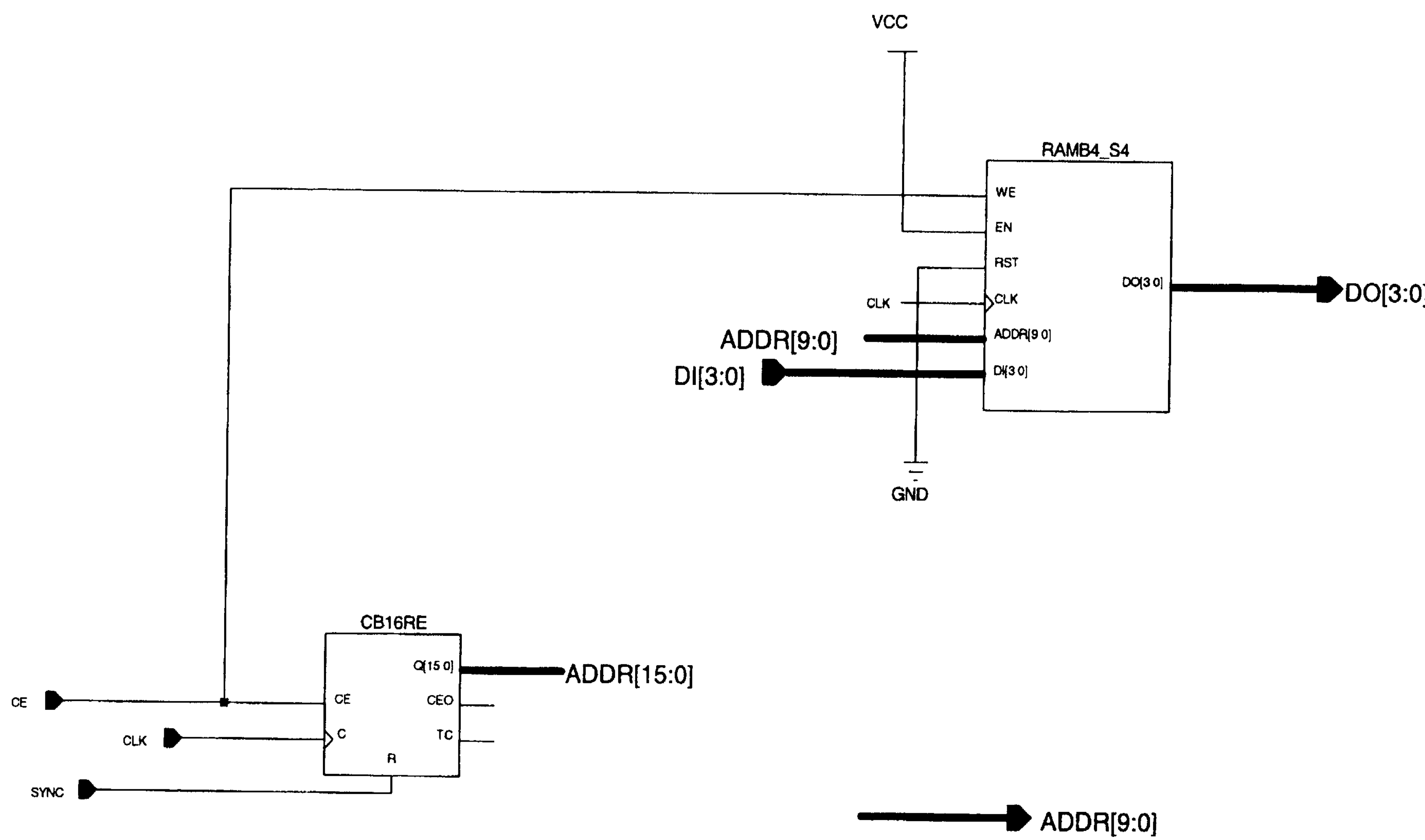
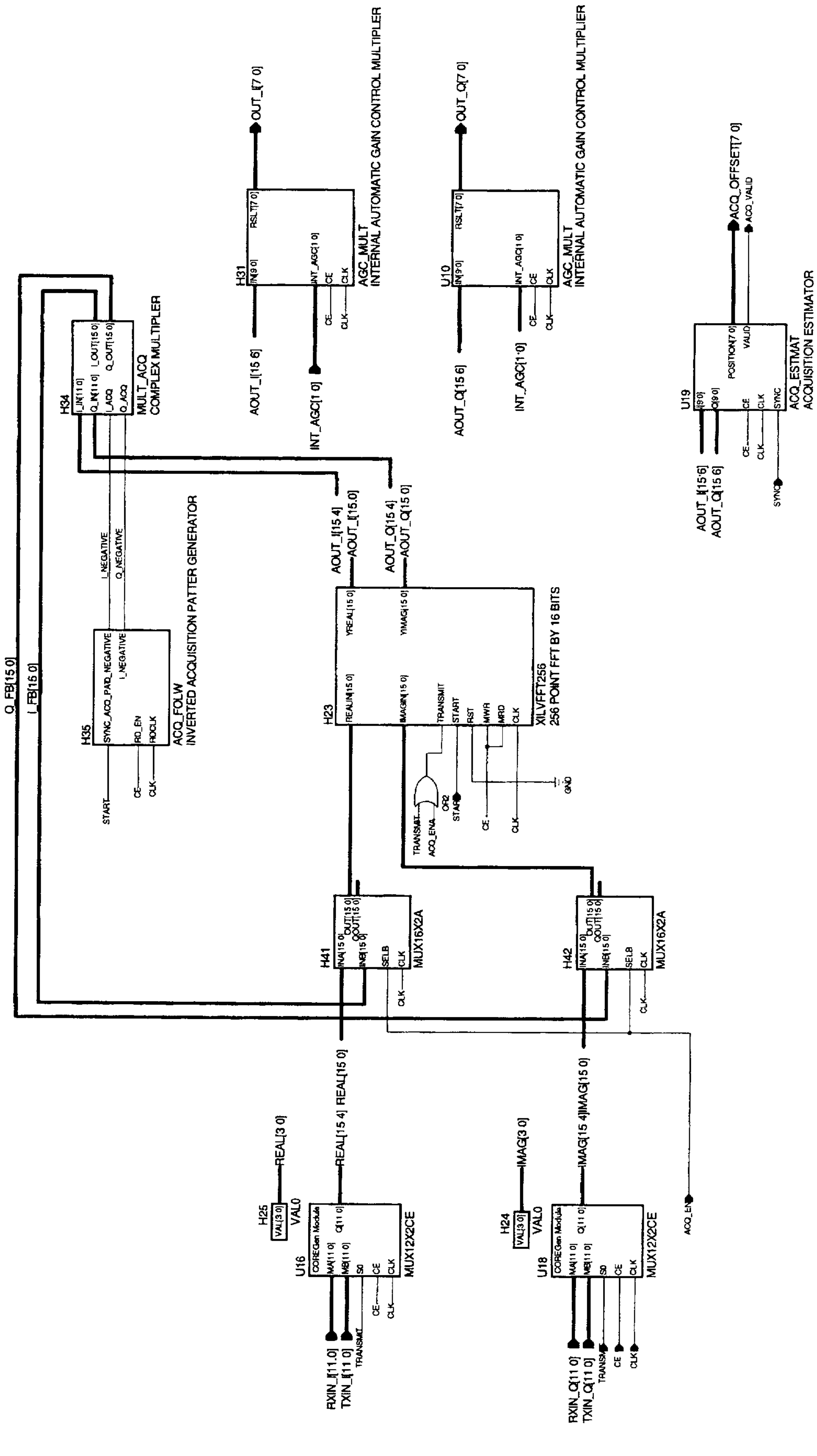
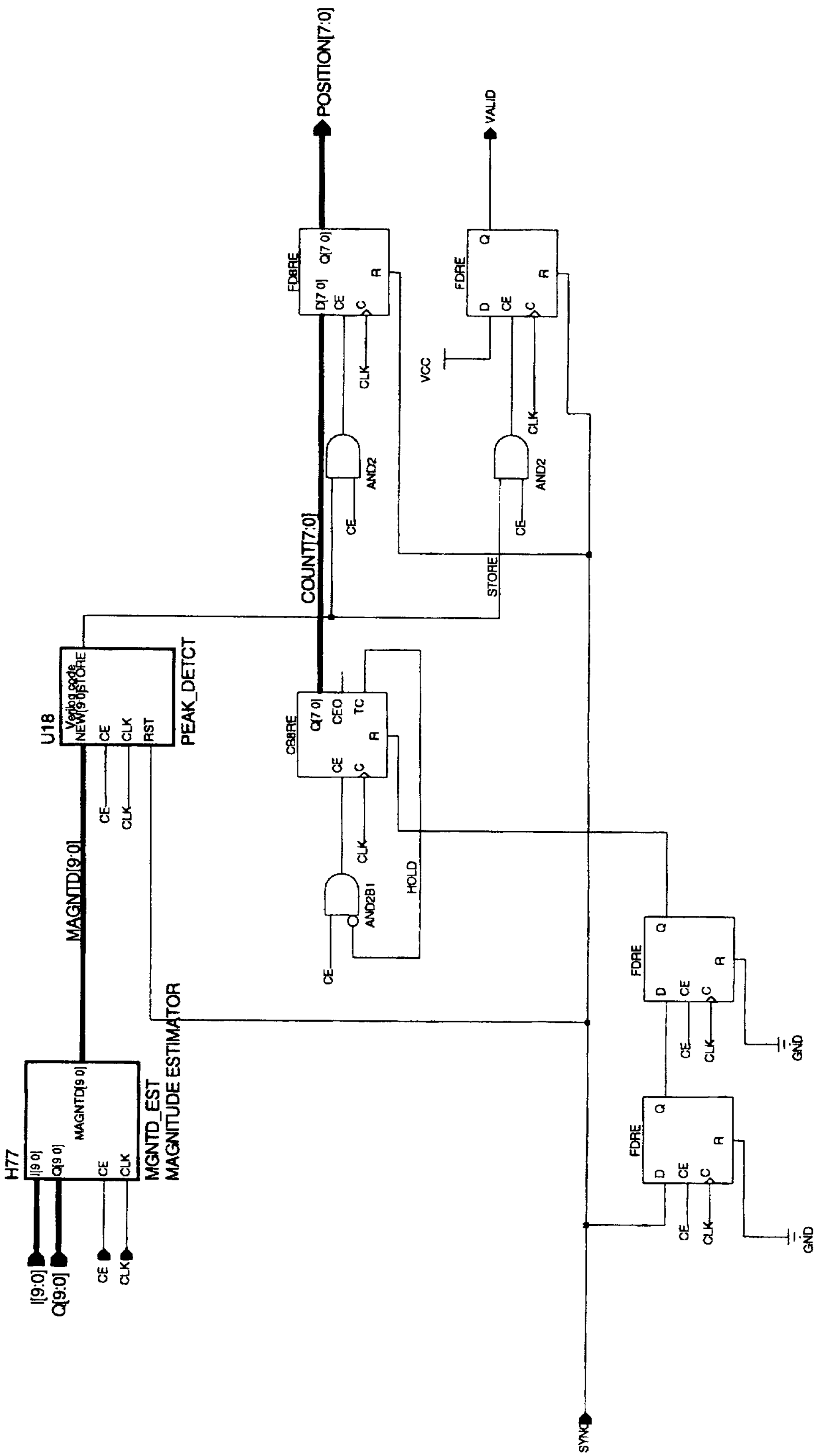

VCC
RAMB4_S4
WE
EN
RST
CLK
ADDR[9:0]
DI[3:0]
DO[3:0]
CLK
ADDR[9:0]
DI[3:0]
DO[3:0]
GND
CB16RE
CE
C
R
Q[15:0]
CEO
TC
ADDR[15:0]
CE
CLK
SYNC
ADDR[9:0]

FIG. 35r



H31
AGC_MULT
INTERNAL AUTOMATIC GAIN CONTROL MULTIPLIER
OUT_I[7:0]
AOUT_I[15:6]
INT_AGC[1:0]
U10
AGC_MULT
INTERNAL AUTOMATIC GAIN CONTROL MULTIPLIER
OUT_Q[7:0]
AOUT_Q[15:6]
INT_AGC[1:0]
U19
ACQ_ESTMAT
ACQUISITION ESTIMATOR
ACQ_OFFSET[7:0]
ACQ_VALID
AOUT_I[15:6]
AOUT_Q[15:6]
SYNC
H34
MULT_ACQ
COMPLEX MULTIPLIER
H35
ACQ_FOLW
INVERTED ACQUISITION PATTER GENERATOR
START
I_NEGATIVE
Q_NEGATIVE
Q_FB[15:0]
I_FB[15:0]
H23
XILVFFT256
256 POINT FFT BY 16 BITS
AOUT_I[15:4]
AOUT_I[15:0]
AOUT_Q[15:4]
AOUT_Q[15:0]
OR2
TRANSMIT
ACQ_ENA
START
GND
H41
MUX16X2A
H42
MUX16X2A
REAL[15:4]
REAL[15:0]
IMAG[15:4]
IMAG[15:0]
H25
VAL0
REAL[3:0]
U16
MUX12X2CE
RXIN_I[11:0]
TXIN_I[11:0]
TRANSMIT
H24
VAL0
IMAG[3:0]
U18
MUX12X2CE
RXIN_Q[11:0]
TXIN_Q[11:0]
ACQ_EN

FIG. 35s



POSITION[7:0]
VALID
FD8RE
D[7:0]
Q[7:0]
CE
C
R
FDRE
D
Q
VCC
CLK
AND2
CE
COUNT[7:0]
STORE
U18
Verilog code
NEW[9:0]
STORE
CLK
RST
PEAK_DETCT
CB8RE
Q[7:0]
CEO
TC
AND2B1
HOLD
MAGNTD[9:0]
H77
I[9:0]
Q[9:0]
MAGNTD[9:0]
MGNTD_EST
MAGNITUDE ESTIMATOR
I[9:0]
Q[9:0]
GND
SYNC

FIG. 35t

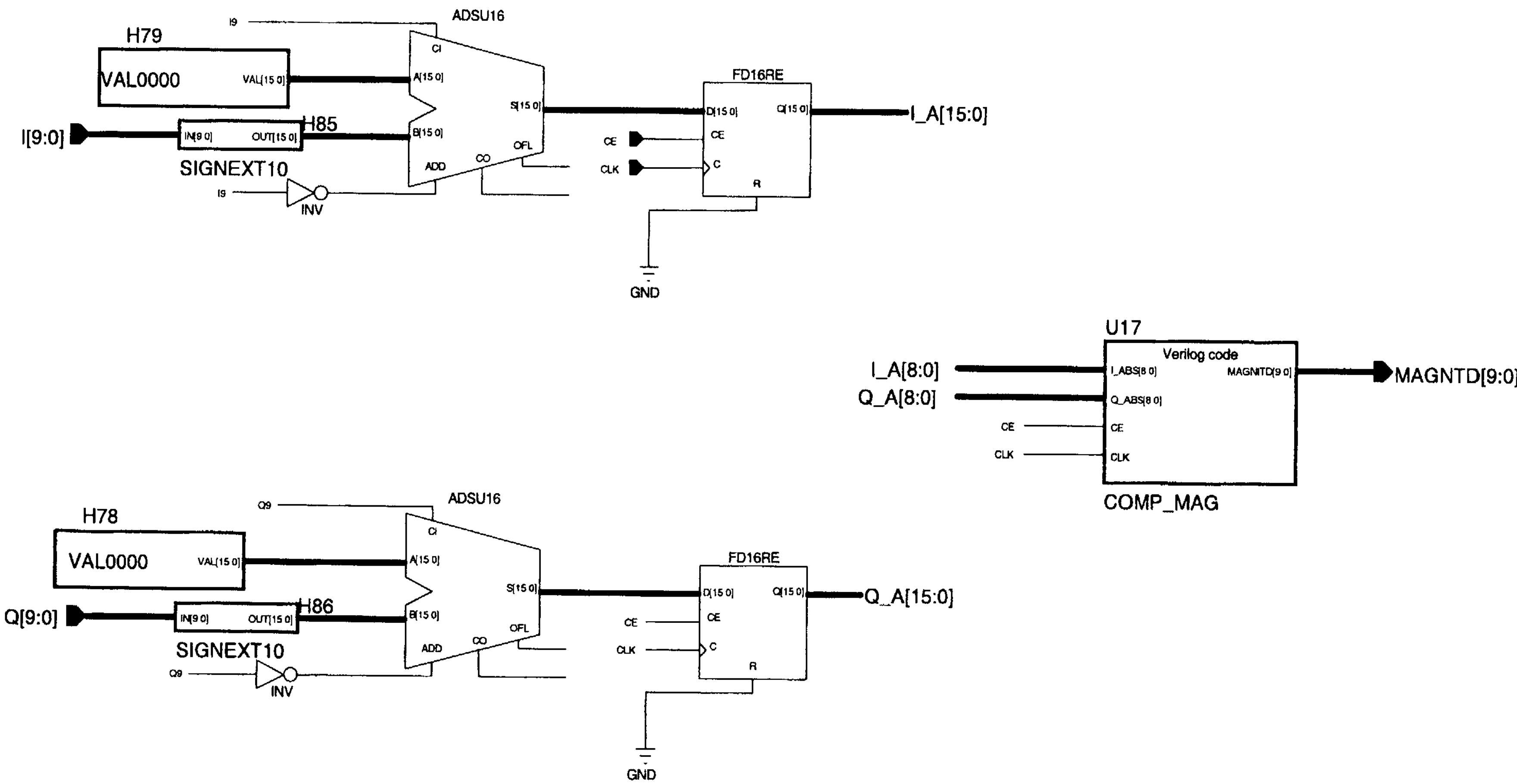

H79
VAL0000
VAL[15:0]
I[9:0]
IN[9:0]
OUT[15:0]
H85
SIGNEXT10
I9
INV
ADSU16
CI
A[15:0]
B[15:0]
ADD
CO
OFL
S[15:0]
FD16RE
D[15:0]
Q[15:0]
CE
C
R
CLK
GND
I_A[15:0]
H78
Q[9:0]
H86
Q9
Q_A[15:0]
U17
Verilog code
I_ABS[8:0]
Q_ABS[8:0]
MAGNTD[9:0]
I_A[8:0]
Q_A[8:0]
MAGNTD[9:0]
COMP_MAG

FIG. 35u

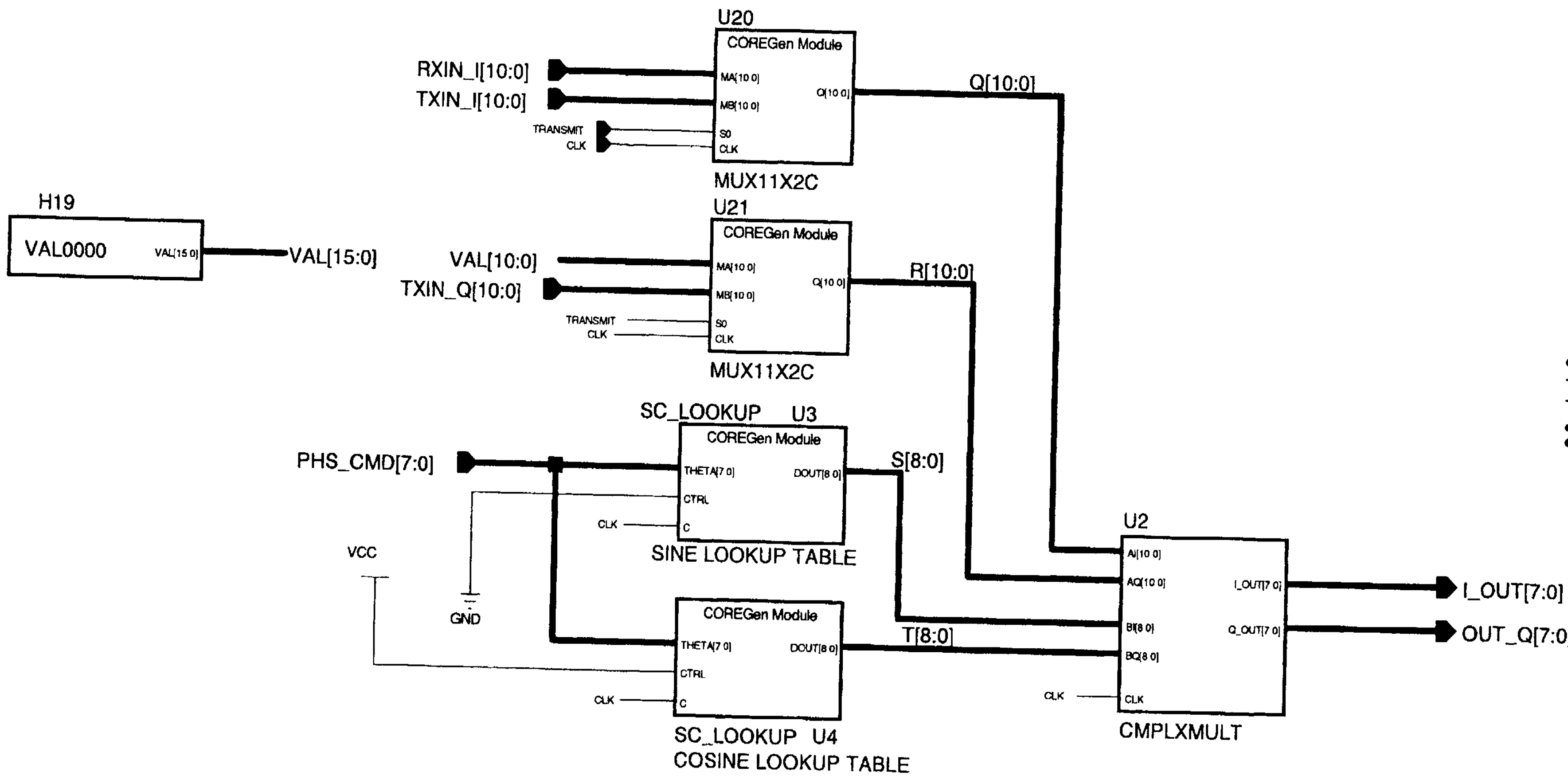

U20
COREGen Module
MA[10 0]
MB[10 0]
S0
CLK
Q[10 0]
MUX11X2C
RXIN_I[10:0]
TXIN_I[10:0]
TRANSMIT
CLK
Q[10:0]
H19
VAL0000
VAL[15 0]
VAL[15:0]
U21
COREGen Module
MA[10 0]
MB[10 0]
S0
CLK
Q[10 0]
MUX11X2C
VAL[10:0]
TXIN_Q[10:0]
TRANSMIT
CLK
R[10:0]
SC_LOOKUP U3
COREGen Module
THETA[7 0]
CTRL
C
DOUT[8 0]
SINE LOOKUP TABLE
PHS_CMD[7:0]
CLK
S[8:0]
VCC
GND
COREGen Module
THETA[7 0]
CTRL
C
DOUT[8 0]
CLK
T[8:0]
SC_LOOKUP U4
COSINE LOOKUP TABLE
U2
AI[10 0]
AQ[10 0]
BI[8 0]
BQ[8 0]
CLK
I_OUT[7 0]
Q_OUT[7 0]
CMPLXMULT
CLK
I_OUT[7:0]
OUT_Q[7:0]

FIG. 35v

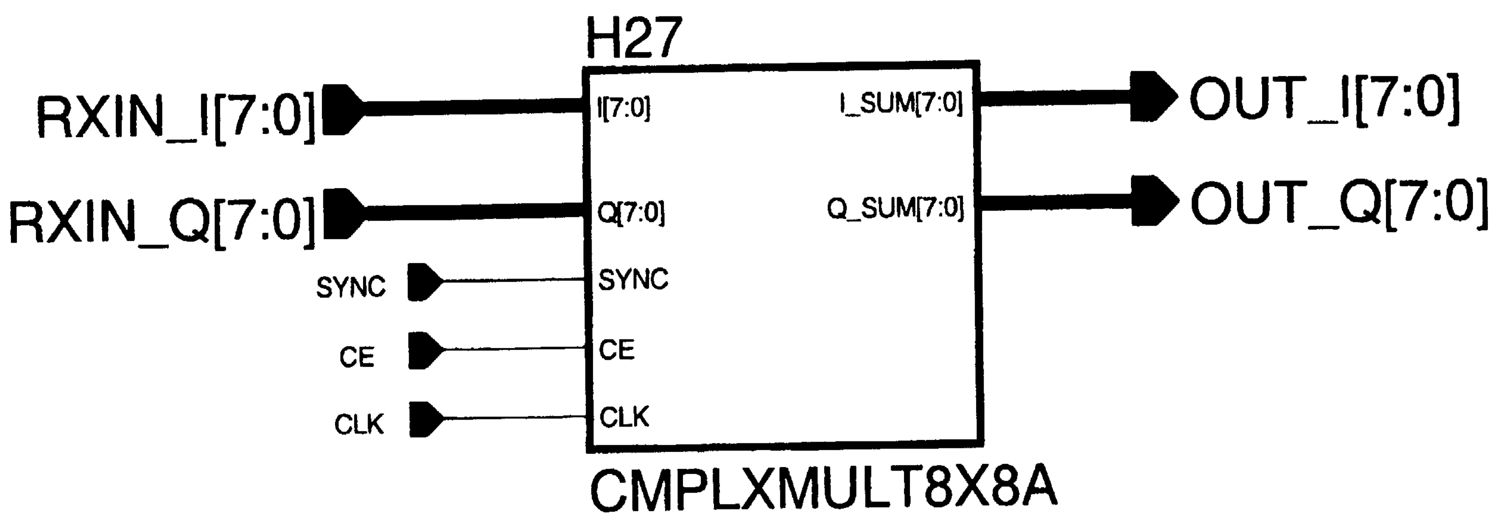
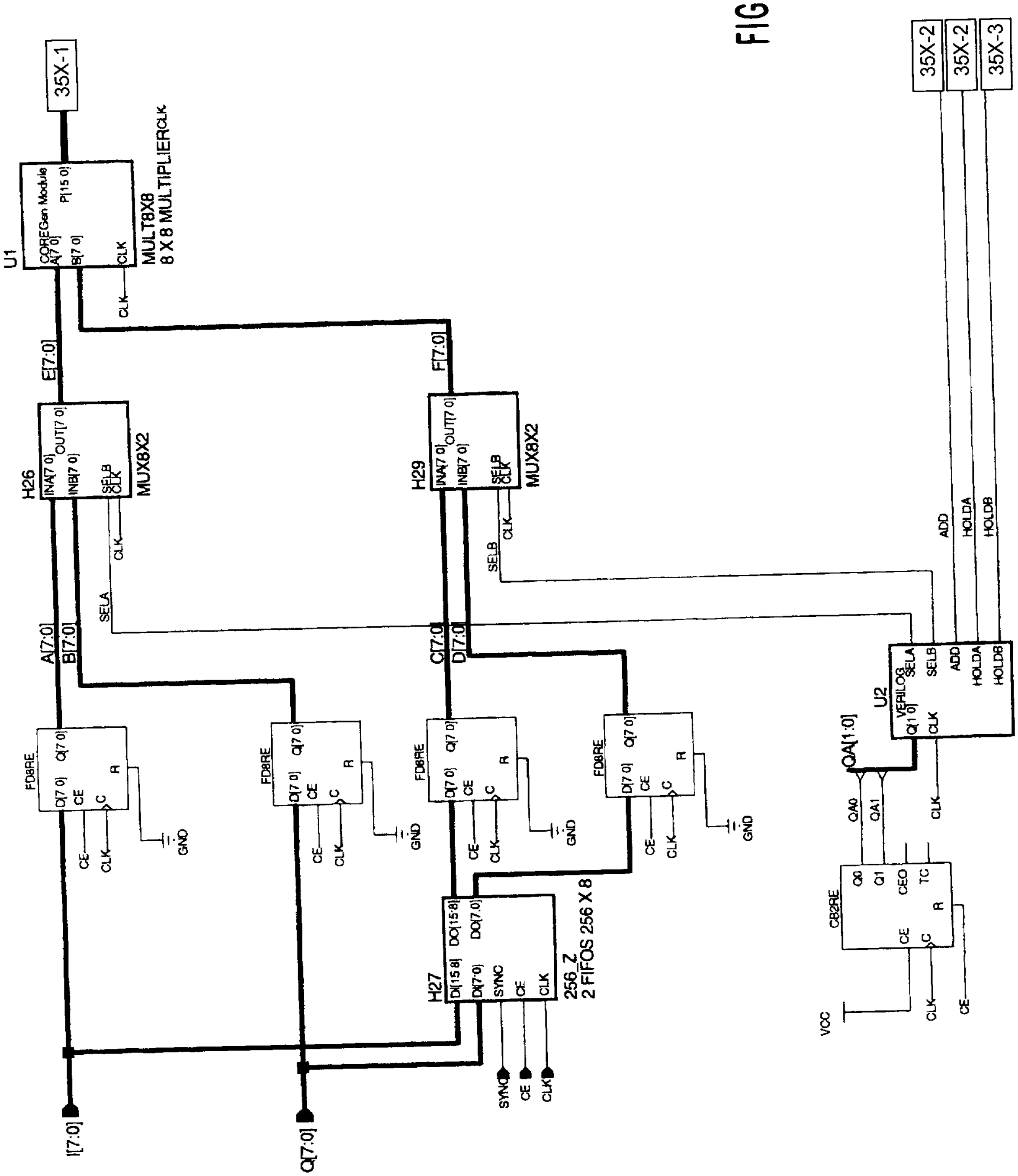

H27
RXIN_I[7:0]
RXIN_Q[7:0]
SYNC
CE
CLK
I[7:0]
Q[7:0]
SYNC
CE
CLK
I_SUM[7:0]
Q_SUM[7:0]
OUT_I[7:0]
OUT_Q[7:0]
CMPLXMULT8X8A

FIG. 35w

FIG. 35x-1


35X-1
U1
COREGen Module
A[7:0]
B[7:0]
CLK
P[15:0]
MULT8X8
8 X 8 MULTIPLIER
E[7:0]
F[7:0]
H26
INA[7:0]
INB[7:0]
OUT[7:0]
SELB
CLK
MUX8X2
H29
MUX8X2
SELA
SELB
A[7:0]
B[7:0]
C[7:0]
D[7:0]
FD8RE
D[7:0]
Q[7:0]
CE
C
R
GND
H27
DI[15:8]
DI[7:0]
DO[15:8]
DO[7:0]
SYNC
256_Z
2 FIFOS 256 X 8
I[7:0]
Q[7:0]
35X-2
35X-2
35X-3
ADD
HOLDA
HOLDB
U2
VERILOG
Q[1:0]
MLTPY_TIM
QA[1:0]
QA0
QA1
CB2RE
Q0
Q1
CEO
TC
VCC

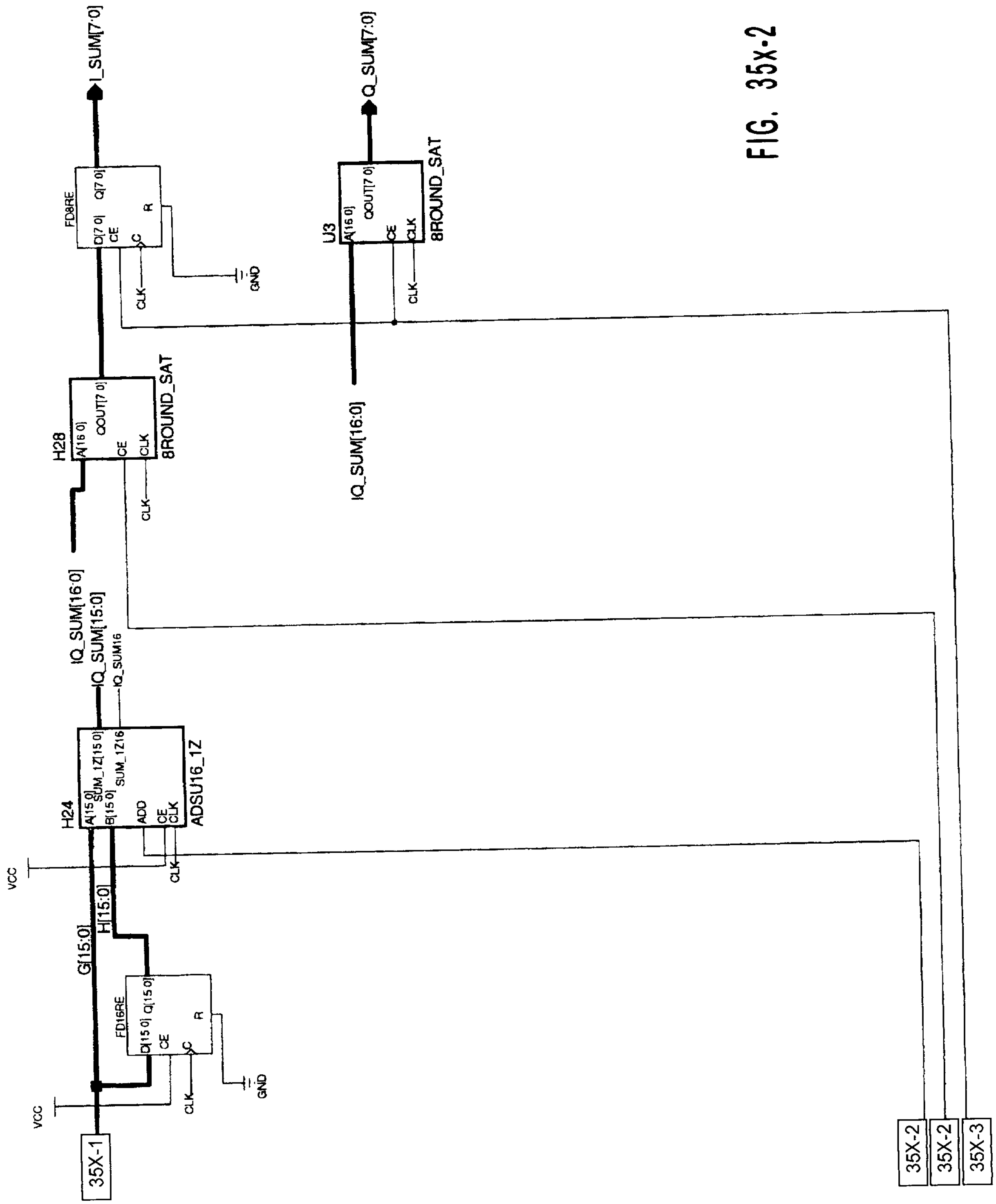
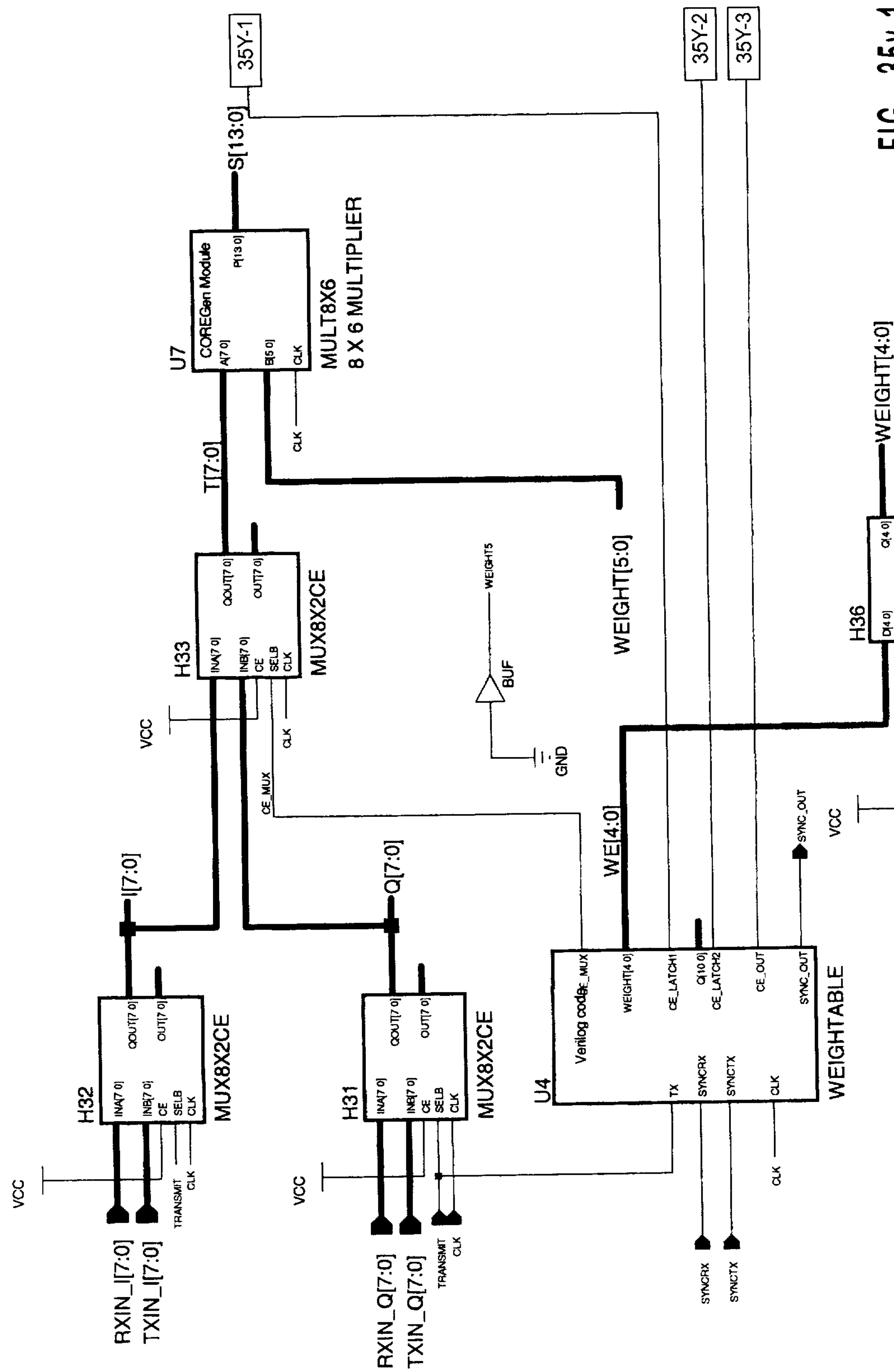

I_SUM[7:0]
Q_SUM[7:0]
FD8RE
D[7:0]
Q[7:0]
CE
C
R
GND
CLK
U3
A[16:0]
QOUT[7:0]
CE
CLK
8ROUND_SAT
H28
A[16:0]
QOUT[7:0]
CE
CLK
8ROUND_SAT
IQ_SUM[16:0]
IQ_SUM[16:0]
IQ_SUM[15:0]
IQ_SUM16
H24
A[15:0]
B[15:0]
SUM_1Z[15:0]
SUM_1Z16
ADD
CE
CLK
ADSU16_1Z
VCC
G[15:0]
H[15:0]
FD16RE
D[15:0]
Q[15:0]
CE
C
R
GND
CLK
VCC
35X-1
35X-2
35X-2
35X-3

FIG. 35x-2



35Y-1
35Y-2
35Y-3
S[13:0]
U7
COREGen Module
MULT8X6
8 X 6 MULTIPLIER
T[7:0]
CLK
WEIGHT[5:0]
H33
MUX8X2CE
VCC
CE_MUX
BUF
GND
WEIGHT5
I[7:0]
Q[7:0]
WE[4:0]
H36
WT_DLY
WEIGHT[4:0]
SYNC_OUT
H32
MUX8X2CE
H31
MUX8X2CE
U4
Verilog code
WEIGHTABLE
RXIN_I[7:0]
TXIN_I[7:0]
RXIN_Q[7:0]
TXIN_Q[7:0]
TRANSMIT
SYNCRX
SYNCTX

FIG. 35y-1

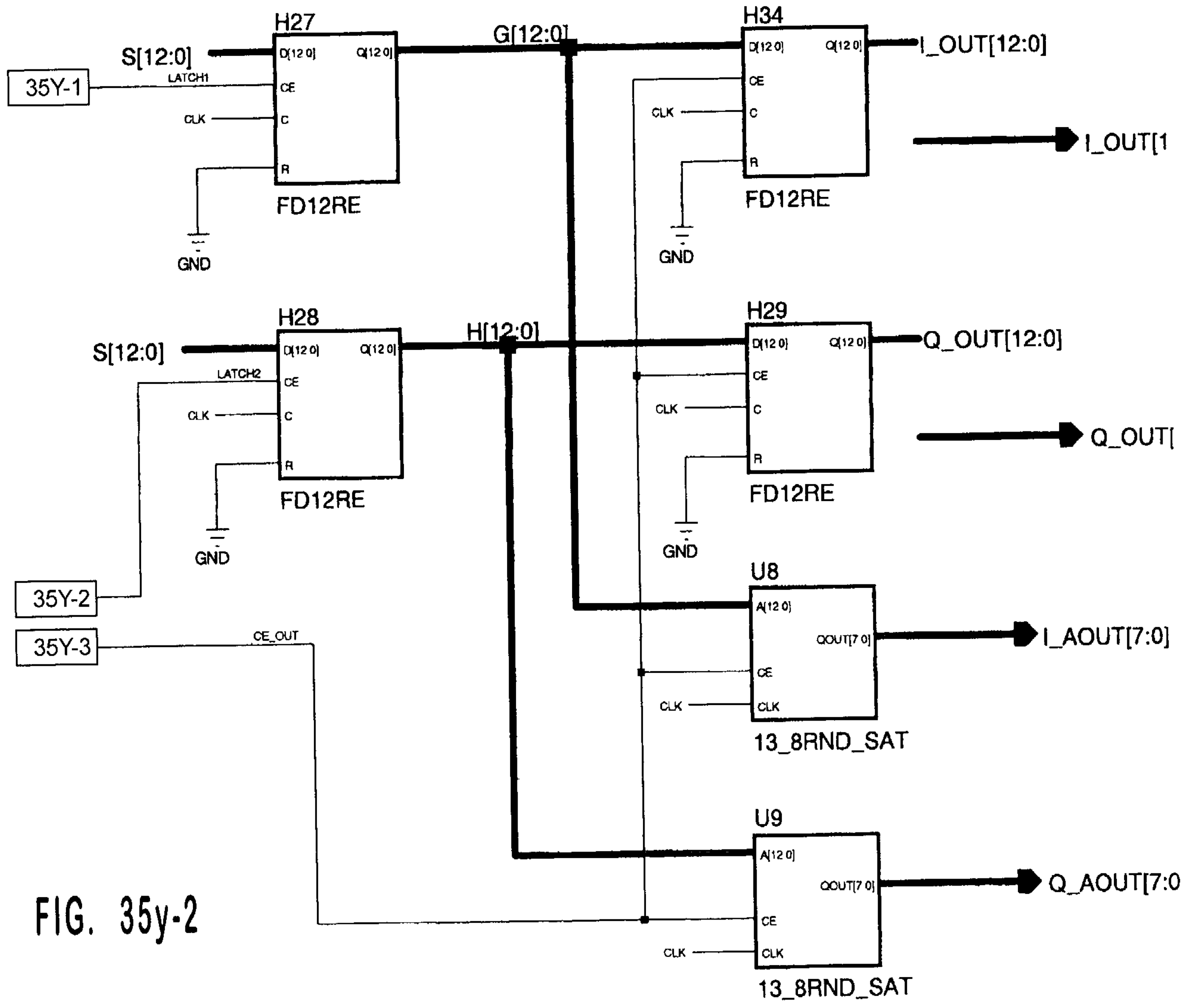

H27
S[12:0]
35Y-1
LATCH1
D[12 0]
Q[12 0]
CE
C
R
CLK
GND
FD12RE
G[12:0]
H34
I_OUT[12:0]
I_OUT[1
FD12RE
H28
S[12:0]
LATCH2
35Y-2
FD12RE
H[12:0]
H29
Q_OUT[12:0]
Q_OUT[
FD12RE
U8
A[12 0]
QOUT[7 0]
I_AOUT[7:0]
13_8RND_SAT
35Y-3
CE_OUT
U9
Q_AOUT[7:0
13_8RND_SAT

FIG. 35y-2

PHASE ACCUMULATOR

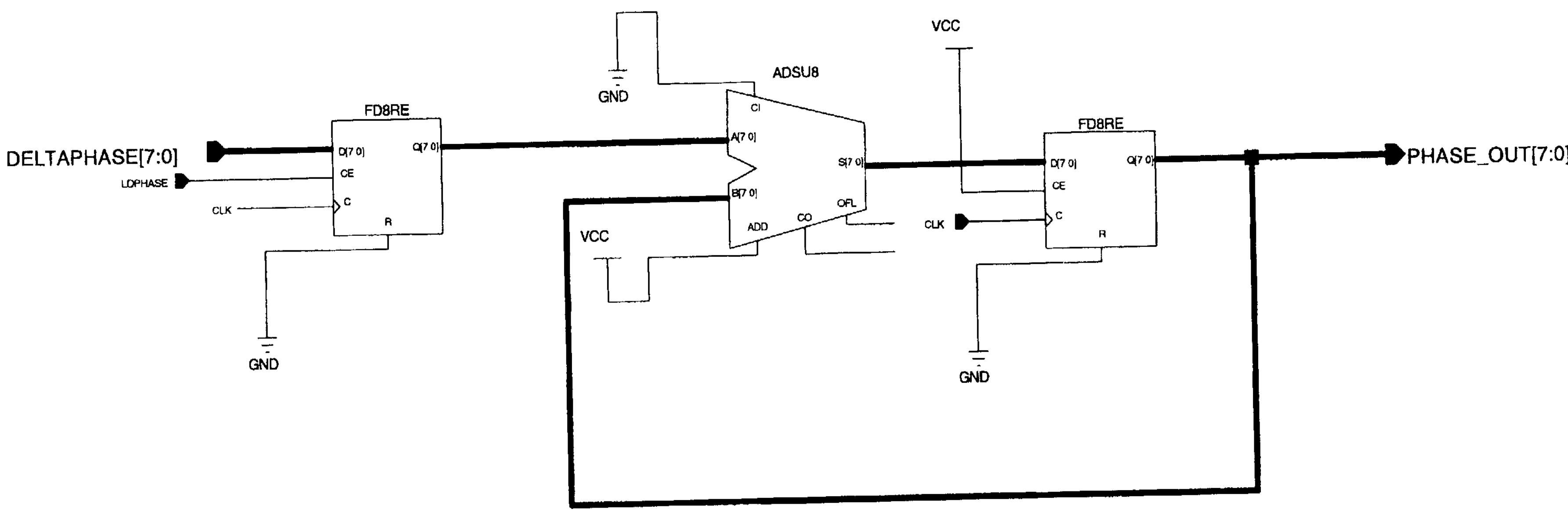


FIG. 35z

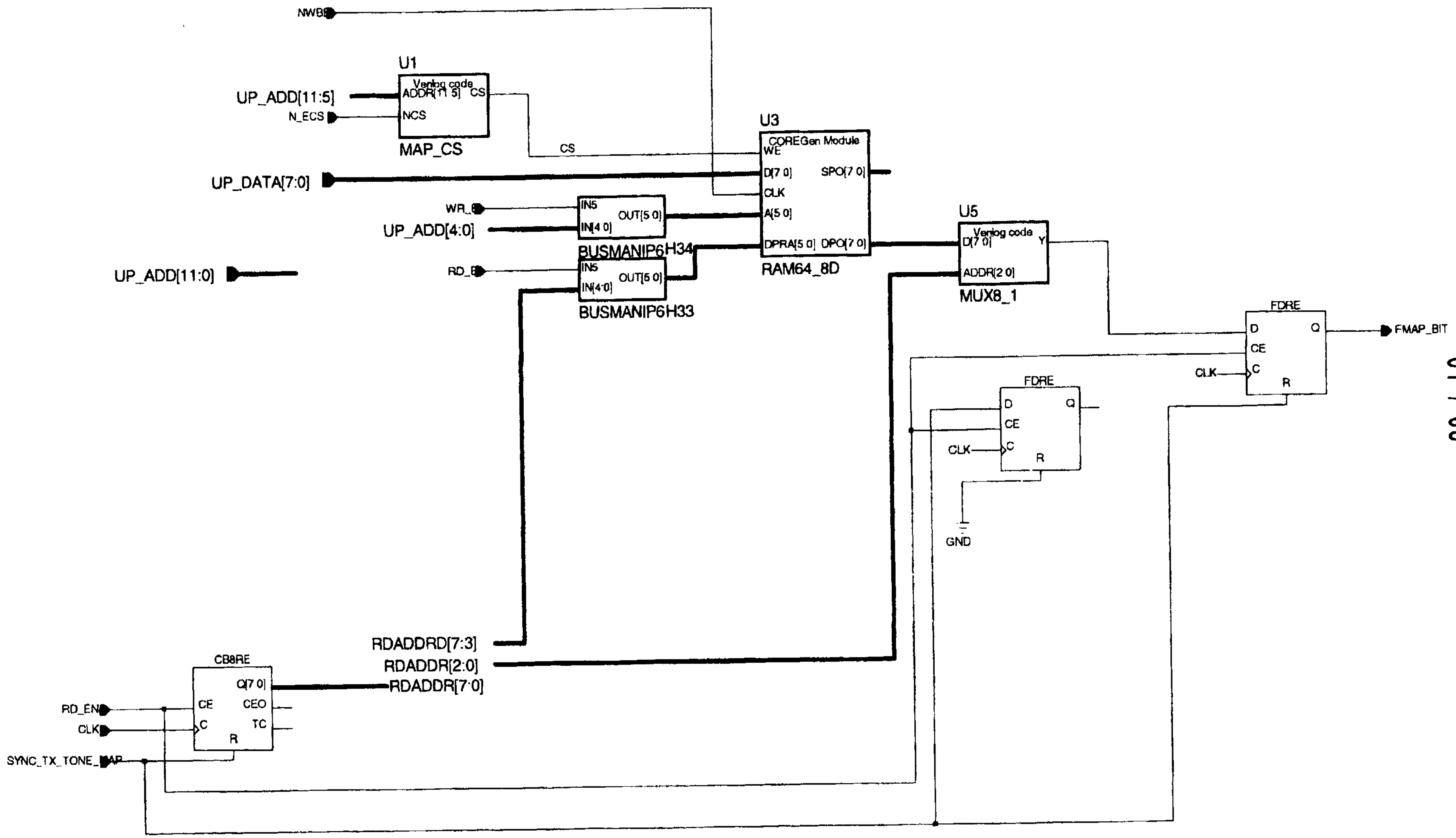

NWBS
U1
Verilog code
ADDR[11:5]
CS
NCS
MAP_CS
UP_ADD[11:5]
N_ECS
CS
UP_DATA[7:0]
U3
COREGen Module
WE
D[7:0]
CLK
A[5:0]
DPRA[5:0]
SPO[7:0]
DPO[7:0]
RAM64_8D
WR_B
UP_ADD[4:0]
IN5
IN[4:0]
OUT[5:0]
BUSMANIP6H34
RD_B
BUSMANIP6H33
UP_ADD[11:0]
U5
Verilog code
D[7:0]
Y
ADDR[2:0]
MUX8_1
FDRE
D
Q
CE
C
R
CLK
FMAP_BIT
GND
RDADDRD[7:3]
RDADDR[2:0]
RDADDR[7:0]
CB8RE
Q[7:0]
CEO
TC
RD_EN
SYNC_TX_TONE_MAP

FIG. 35aa

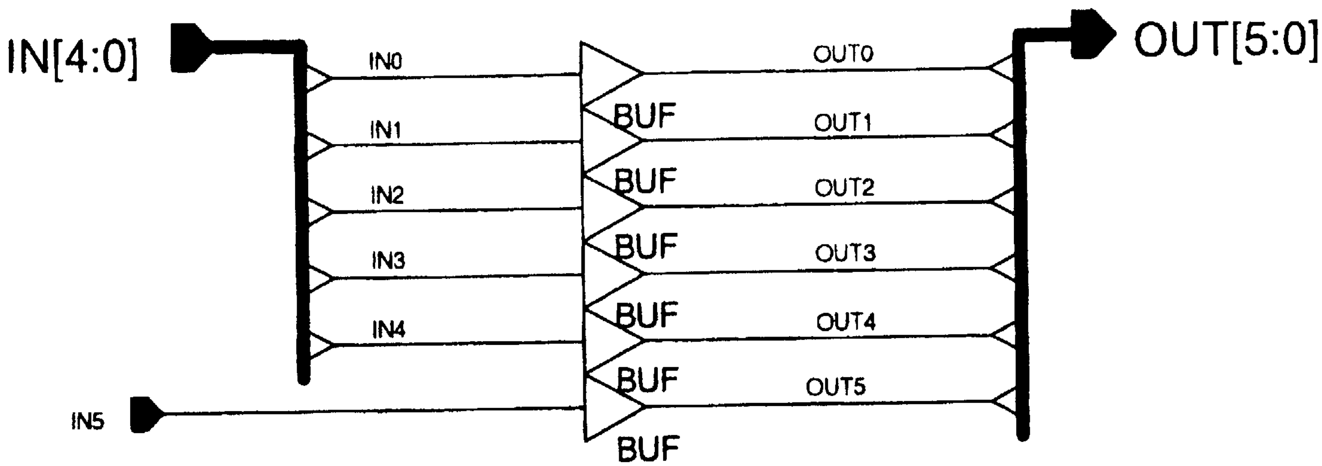

IN[4:0]
IN0
IN1
IN2
IN3
IN4
IN5
BUF
BUF
BUF
BUF
BUF
BUF
OUT0
OUT1
OUT2
OUT3
OUT4
OUT5
OUT[5:0]

FIG. 35ab

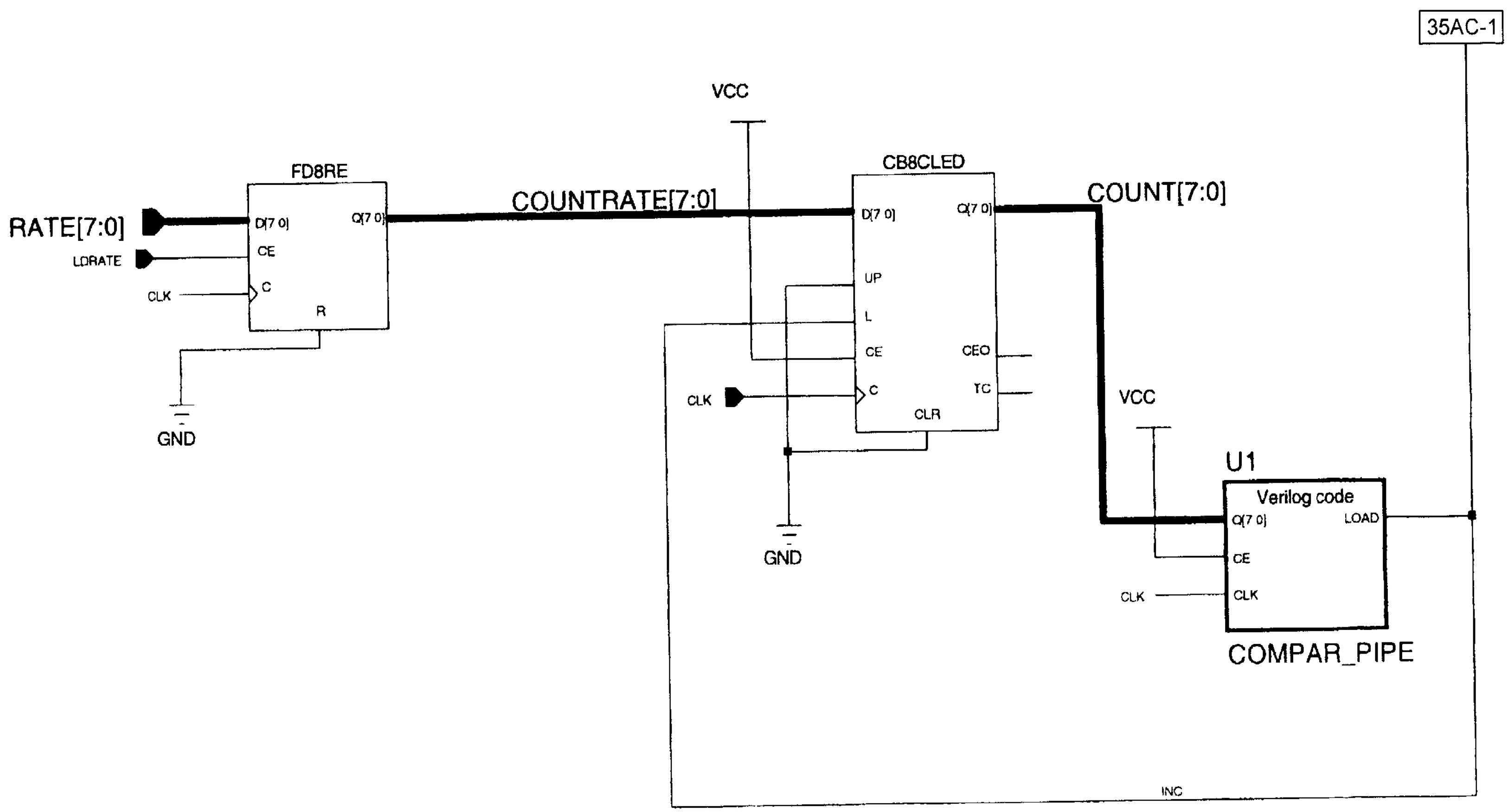

35AC-1
VCC
FD8RE
CB8CLED
RATE[7:0]
D[7 0]
Q[7 0]
COUNTRATE[7:0]
D[7 0]
Q[7 0]
COUNT[7:0]
LDRATE
CE
CLK
C
R
UP
L
CE
CEO
CLK
C
TC
CLR
GND
VCC
GND
U1
Verilog code
Q[7 0]
LOAD
CE
CLK
CLK
COMPAR_PIPE
INC

FIG. 35ac-1

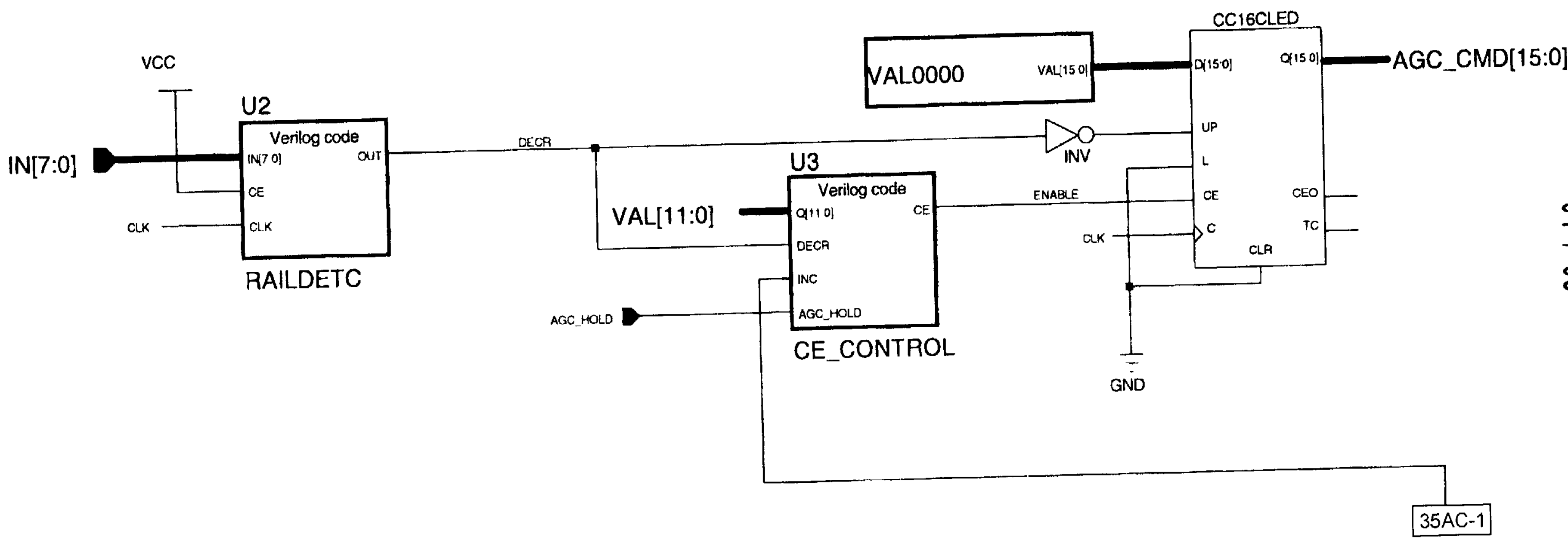

VCC
U2
Verilog code
IN[7:0]
IN[7 0]
CE
CLK
OUT
CLK
RAILDETC
DECR
VAL[11:0]
U3
Verilog code
Q[11 0]
DECR
INC
AGC_HOLD
CE
AGC_HOLD
CE_CONTROL
VAL0000
VAL[15 0]
INV
ENABLE
CLK
GND
CC16CLED
D[15:0]
UP
L
CE
C
CLR
Q[15 0]
CEO
TC
AGC_CMD[15:0]
35AC-1

FIG. 35ac-2

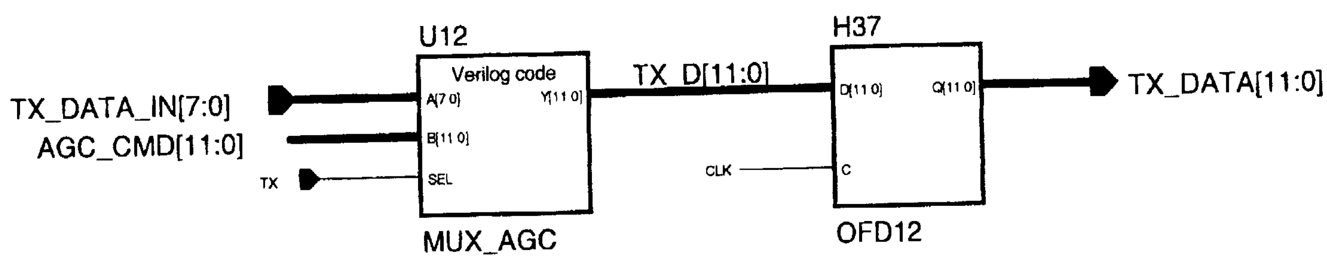

U12
Verilog code
A[7 0]
B[11 0]
SEL
Y[11 0]
MUX_AGC
TX_DATA_IN[7:0]
AGC_CMD[11:0]
TX
TX_D[11:0]
H37
D[11 0]
Q[11 0]
C
CLK
OFD12
TX_DATA[11:0]

FIG. 35ac-3

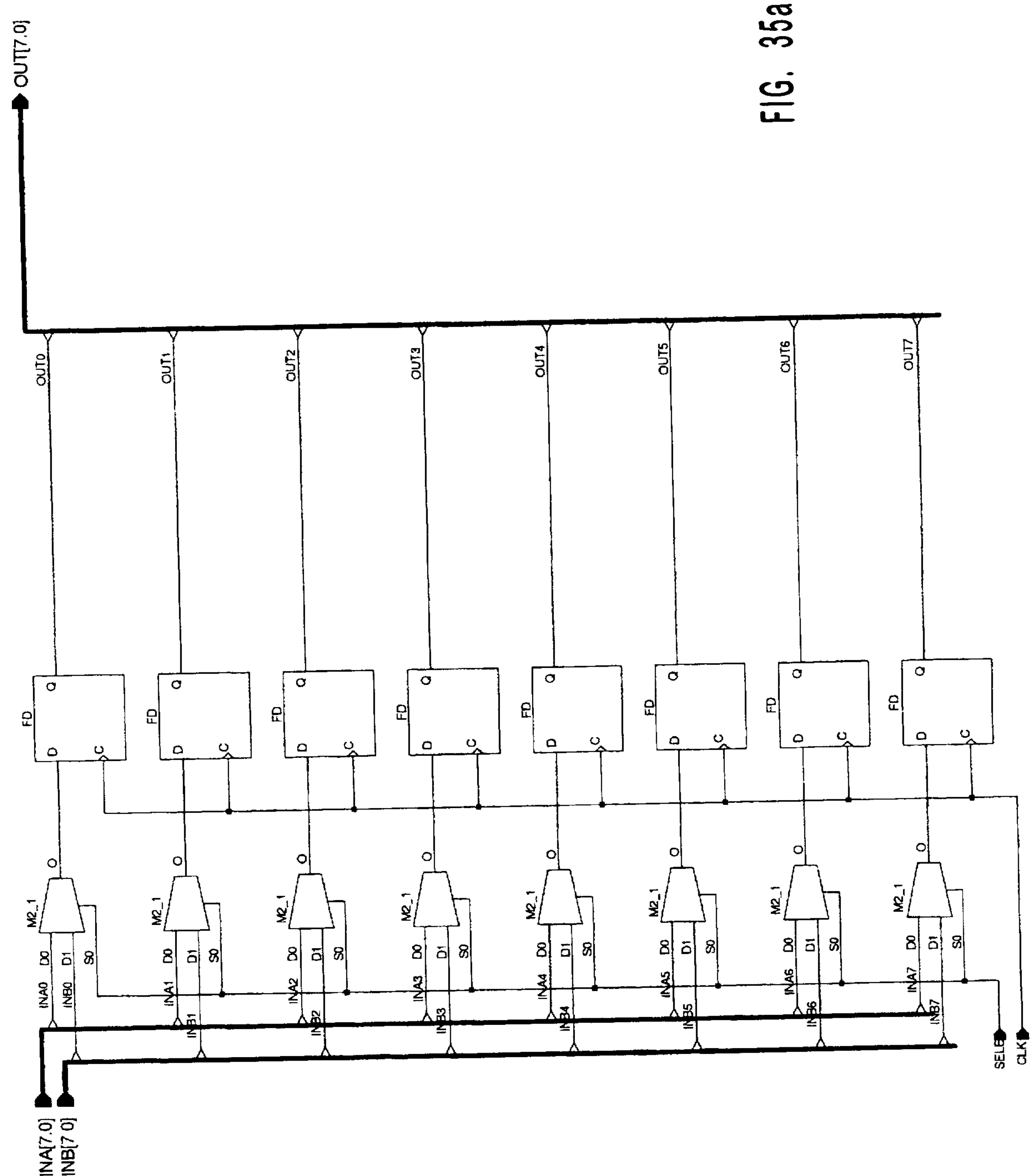

OUT[7:0]
OUT0
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
FD
D
C
Q
M2_1
D0
D1
S0
O
INA0
INB0
INA1
INB1
INA2
INB2
INA3
INB3
INA4
INB4
INA5
INB5
INA6
INB6
INA7
INB7
INA[7:0]
INB[7:0]
SELB
CLK

FIG. 35ad

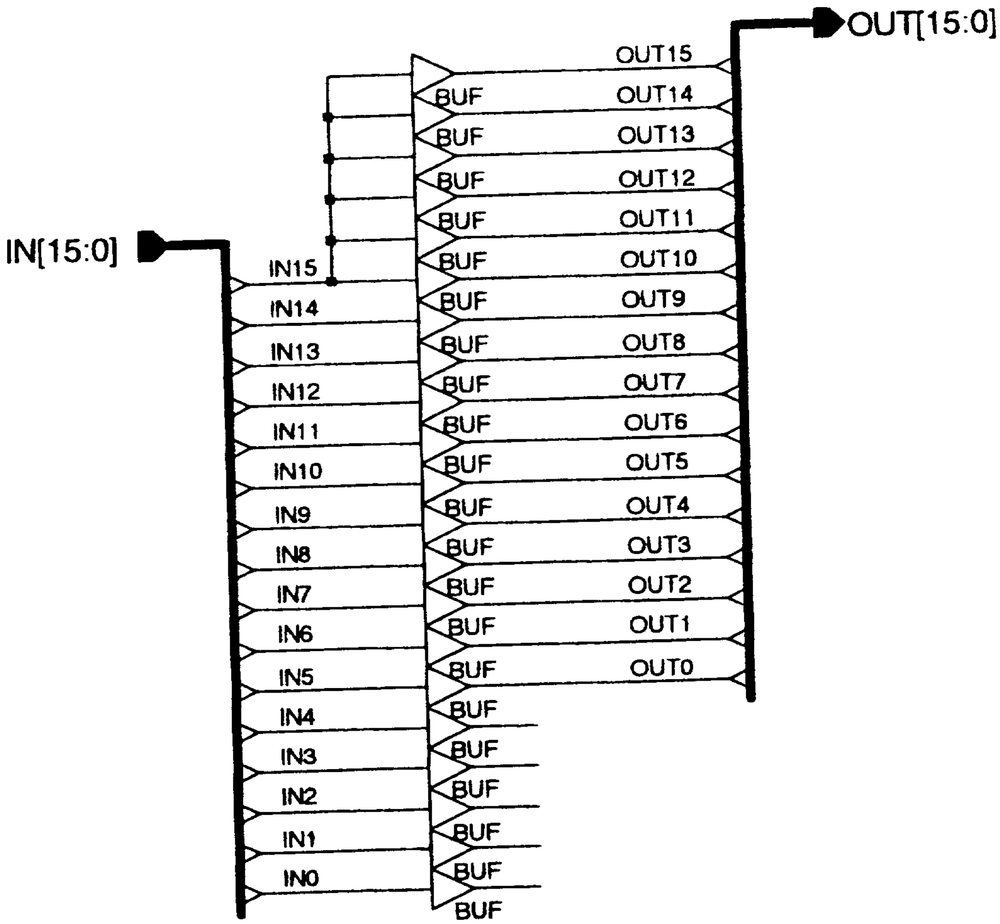

OUT[15:0]
IN[15:0]
OUT15
OUT14
OUT13
OUT12
OUT11
OUT10
OUT9
OUT8
OUT7
OUT6
OUT5
OUT4
OUT3
OUT2
OUT1
OUT0
IN15
IN14
IN13
IN12
IN11
IN10
IN9
IN8
IN7
IN6
IN5
IN4
IN3
IN2
IN1
IN0
BUF

FIG. 35ae

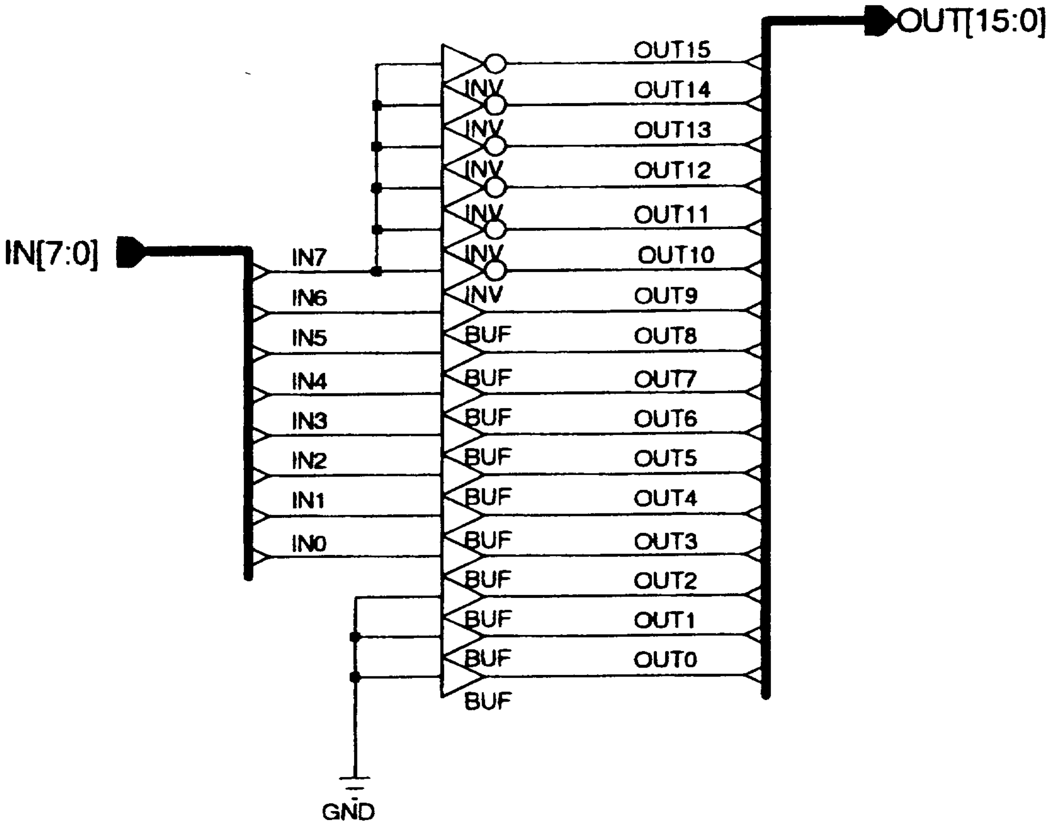

OUT[15:0]
IN[7:0]
IN7
IN6
IN5
IN4
IN3
IN2
IN1
IN0
INV
INV
INV
INV
INV
INV
INV
BUF
BUF
BUF
BUF
BUF
BUF
BUF
BUF
BUF
OUT15
OUT14
OUT13
OUT12
OUT11
OUT10
OUT9
OUT8
OUT7
OUT6
OUT5
OUT4
OUT3
OUT2
OUT1
OUT0
GND

FIG. 35af